Control IC

for quasi-resonant power supply

MS1003SH/MS1004SH

Application Note

The product and product specifications are subject to change without notice.

SHINDENGEN

SHINDENGEN ELECTRIC MFG. CO. , LTD

Precautions

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Warning		Improper handling may result in death, serious injury, or major property damage.
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Warning		This IC is intended to be used for general electronic equipment (office equipment, communication equipment, measurement equipment, consumer electronics, etc.). Do not use the product for medical equipment, aerospace planes, trains, transportation equipment (vehicles, ships, etc.), or nuclear power control systems that may directly affect human life or health in case of a malfunction or trouble. Contact us before using the product in applications other than general electronic equipment.
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		In the event of a problem, an excessive voltage may arise at an output terminal, or the voltage may drop. Anticipate these fluctuations and any consequential malfunctions or destruction and provide adequate protection for equipment, such as overvoltage or overcurrent protection.
		Check the polarity of the input and output terminals. Make sure they are properly connected before turning on power. <<Failure to do so may lead to failure of the protective element or generate smoke or fire.>>
		Use only the specified input voltage. Deploy a protective element on the input line. <<Problems may result in smoke or fire.>>
		In the event of a malfunction or other anomaly, shut power off and contact us immediately.

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Special applications
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Specific applications
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Contents

1. Overview

1.1 Introduction

We have developed the MS1003SH and MS1004SH to meet the growing demand for power conservation. These ICs incorporate a super standby mode to optimize power efficiency under micro loads.

The MS1003SH and MS1004SH consume less power in standby mode than conventional ICs. The ICs incorporate various functions to make it more user-friendly and to make it easier to design a power supply with fewer external components.

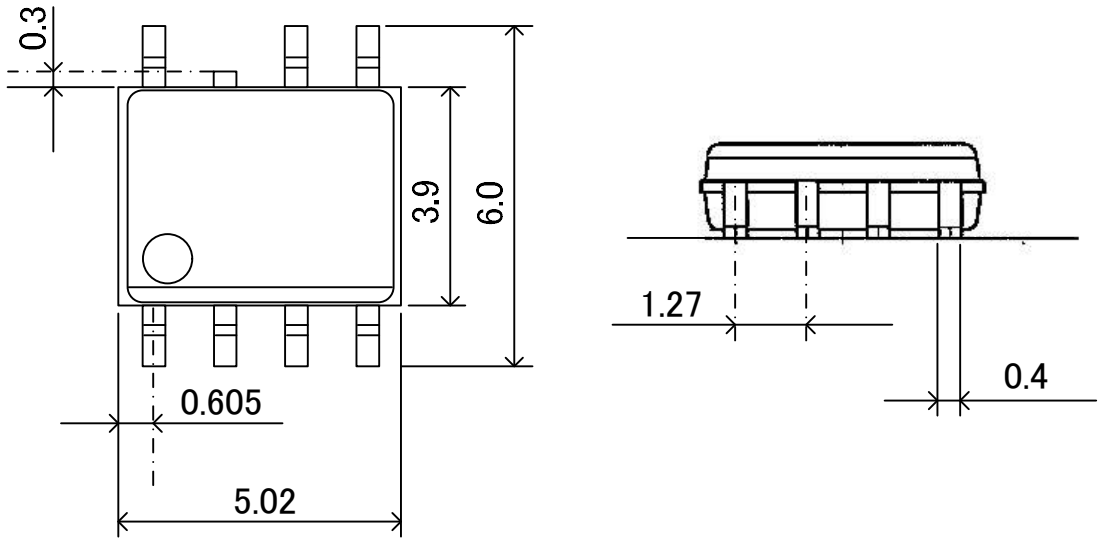
1.2 Characteristics

1) Quasi-resonant design for high efficiency and low noise
2) Four-step soft-start function
3) Onboard startup circuit requires no startup resistor, dramatically reducing losses in the startup circuit.
4) The automatic bottom-skip function controls increases in oscillation frequency and improves efficiency under light loads.
5) Auto-burst mode improves efficiency under light loads with no additional components.
6) Super-standby mode improves efficiency under micro loads.
7) Soft drive circuit reduces noise.
8) Thermal shutdown, overvoltage protection, and overload protection (Timer latch)
9) Primary current limit circuit incorporates an input voltage dependence correction circuit to reduce the number of components required.
10) Bias assist function for startup circuit.
11) VCC-GND short circuit protection function
12) SOP-8/7J package employed for compact dimensions

1.3 Applications

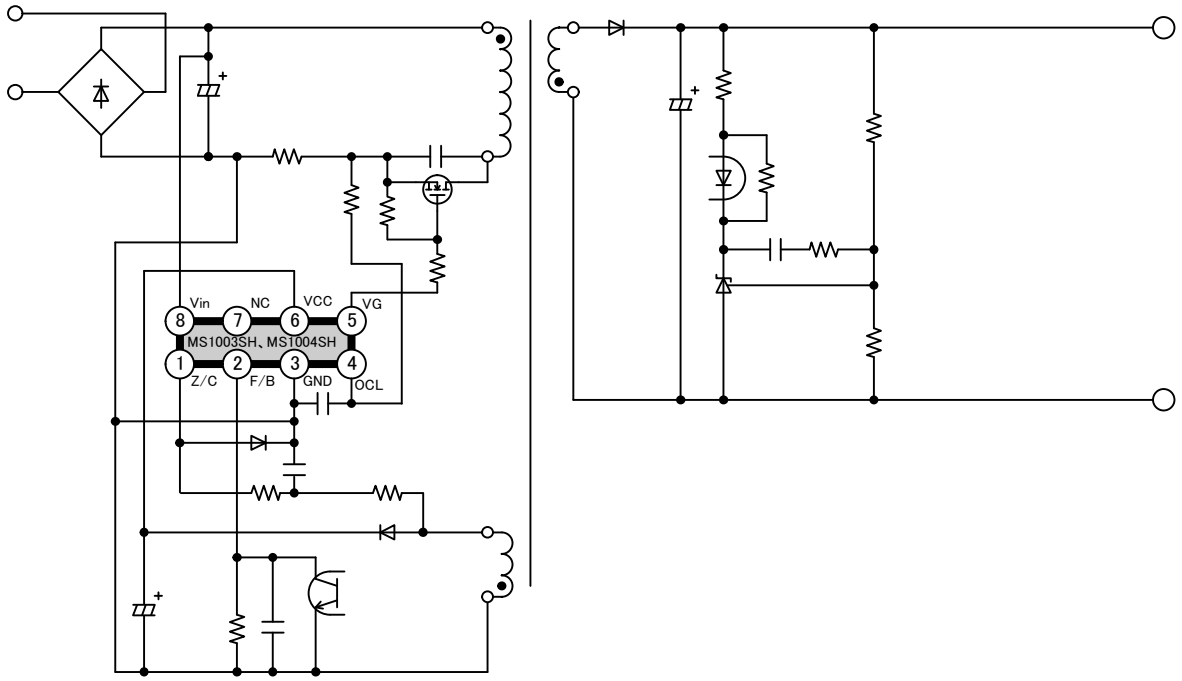
Industrial equipment, video recorders, refrigerators, washing machines, air conditioners and other appliances in which standby power consumption is a design goal.

1.4 Package outline and dimensions Unit: mm

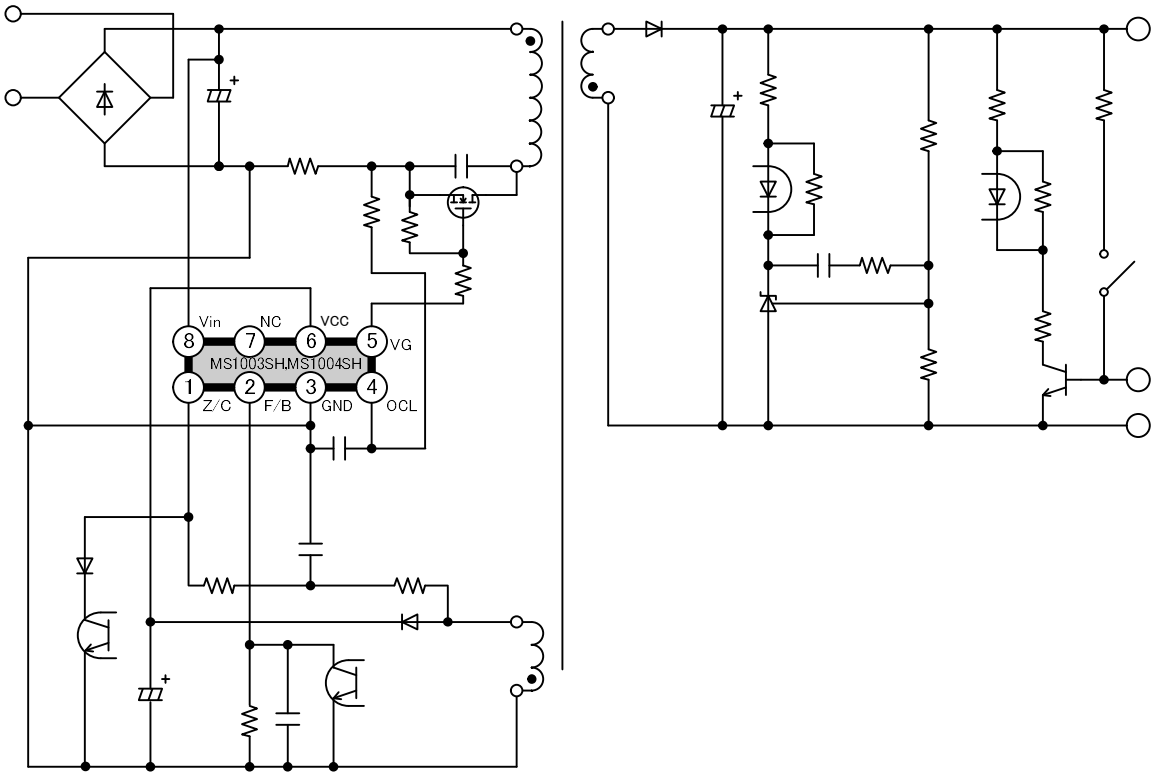


1.5 Basic circuit configuration

(1) Circuit without super-standby mode (Only auto-burst mode is used)

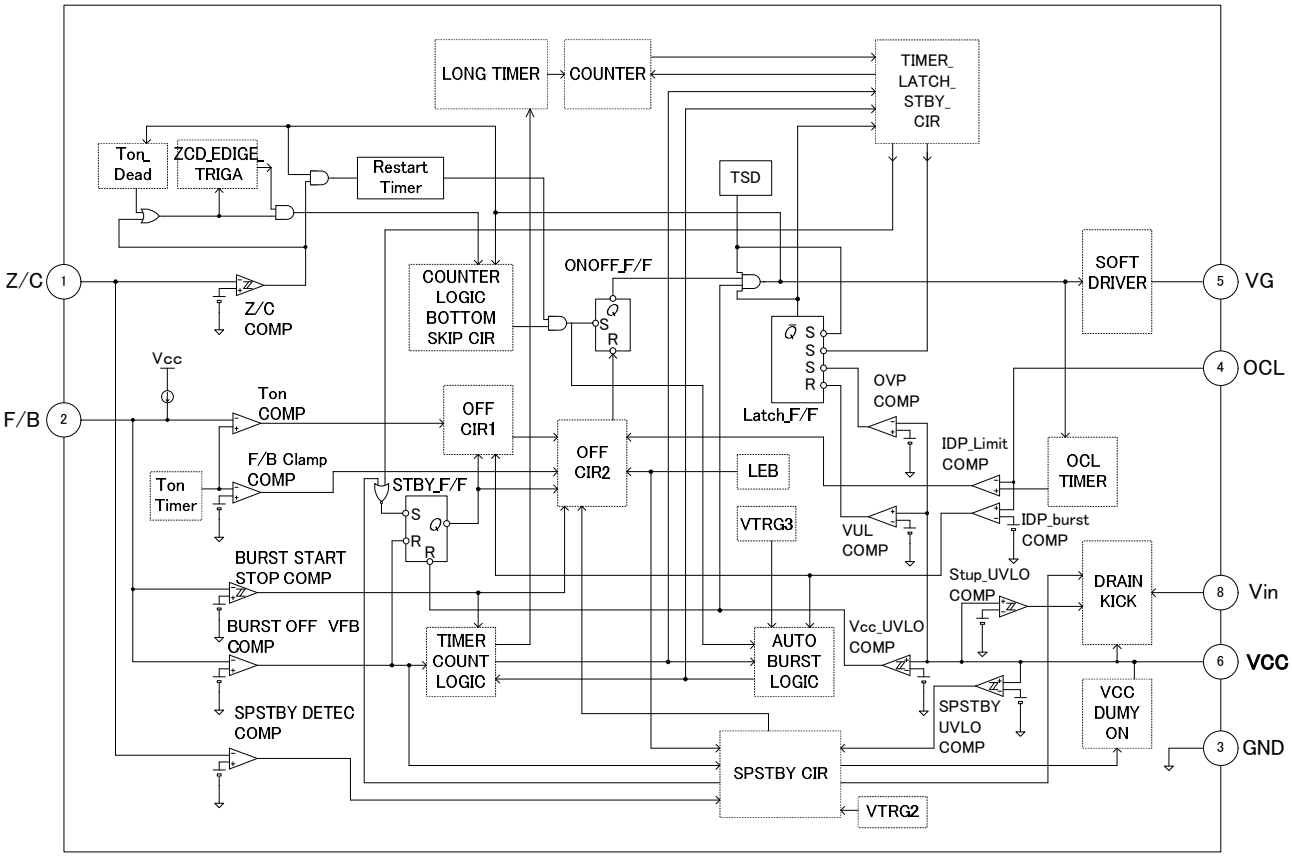


(2) Circuit with super standby mode

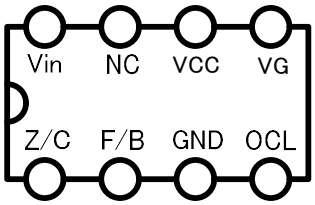


2. Block diagram

2.1 Block diagram



2.2 Pin names

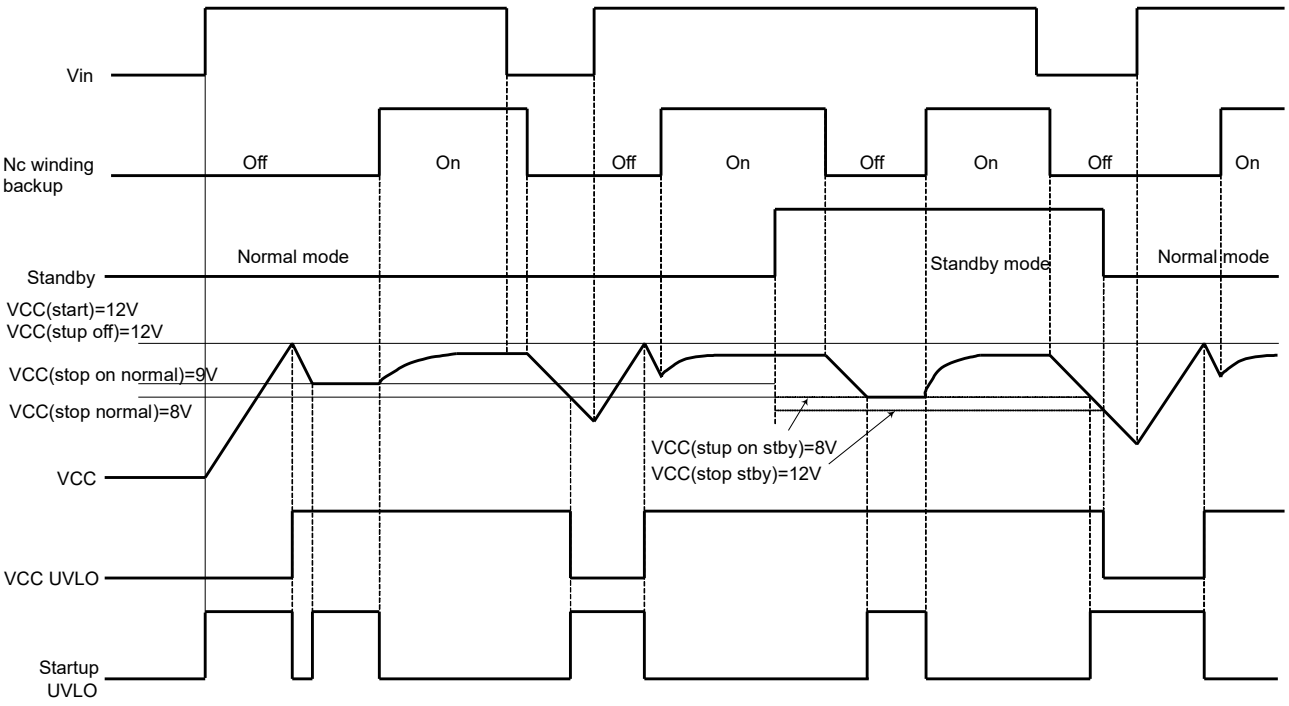


Pin number	Symbol	Pin name
1	Z/C	Zero current detection pin
2	F/B	Feedback signal input pin
3	GND	Ground pin
4	OCL	Overcurrent limit pin
5	VG	VG pin
6	VCC	VCC pin
7	NC	No connection
8	Vin	Vin pin

3. Circuit operation

3.1 Startup

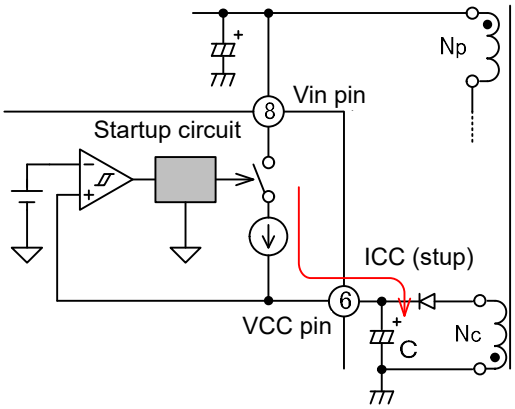
The diagram below shows the startup sequence.



Startup sequence

3.1.1 Startup circuit

The startup circuit does not require a startup resistor, making it possible to easily start the IC with a small number of components. A schematic diagram of the startup circuit is shown to the right.



Until the IC starts up, the startup circuit current ICC(stup) flows from the Vin pin to the VCC pin to charge C, as shown in the diagram.

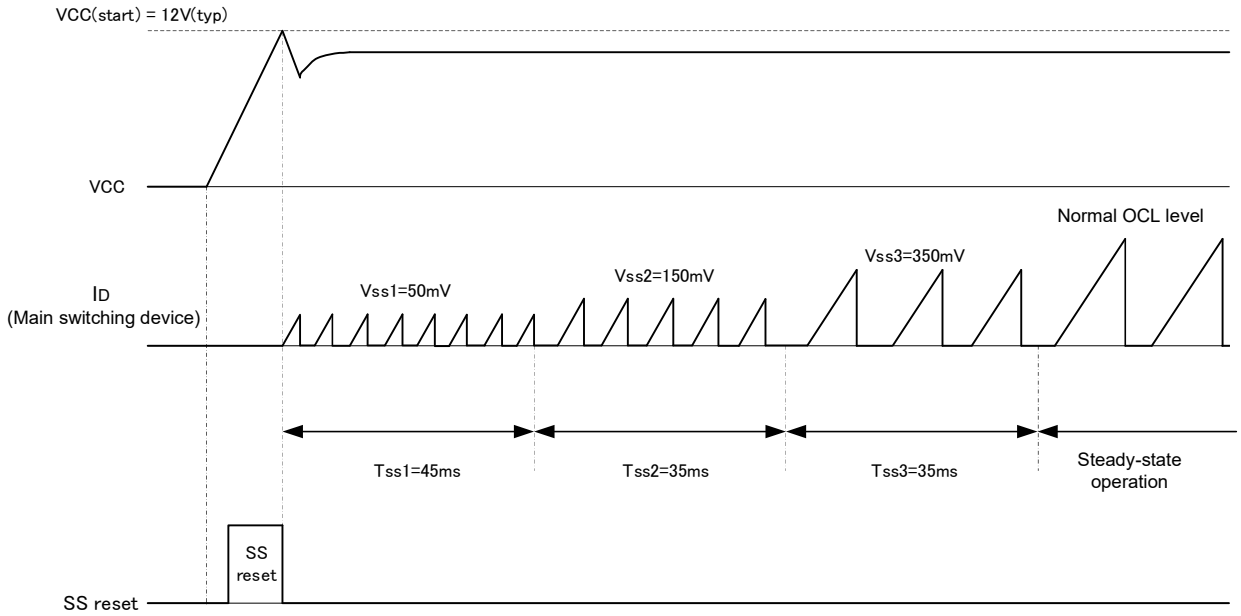
Oscillation begins when the voltage at the VCC pin : VCC reaches"On-State voltage" (VCC (start)) = 12 V (typ). The startup circuit opens, and the startup circuit current stops. The VCC pin has hysteresis, which begins oscillating at VCC (start) and stops oscillating at "Under-Voltage lockout"(VCC (stop stby)) = 7 V(typ) or (VCC (stop normal)) = 8 V (typ).

A bias assist function is provided for the VCC voltage to ensure safe startup. For more information on the bias assist function, see Section 3.1.3.

3.1.2 Soft start (SS)

At startup, the OCL level changes in four stages. Current flowing to the main switch also increases in stages. The envelope curves of the current to the main switch are shaped in four steps to avoid abrupt switch startups.

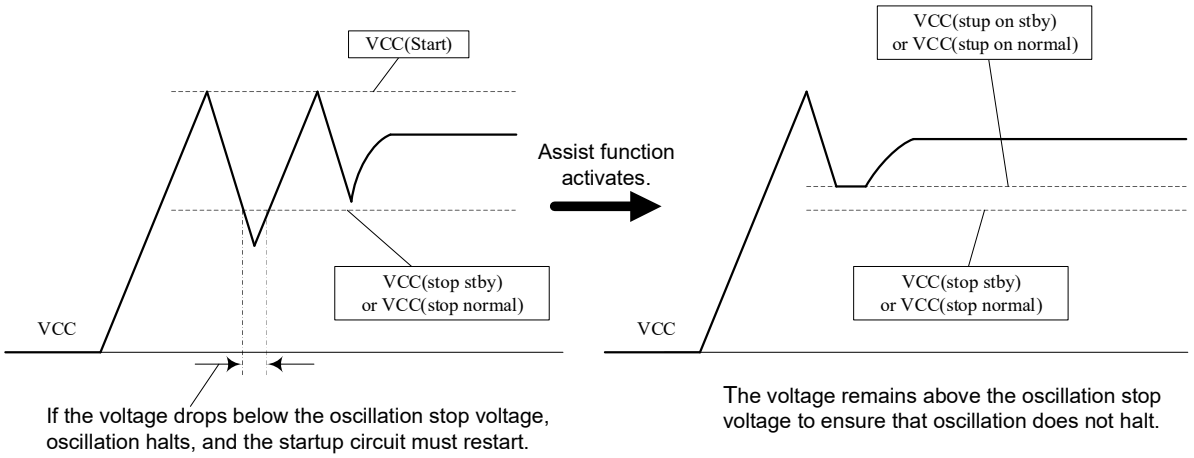
The soft start time depends on ”SS time” (Tss1) to (Tss3) settings. The time settings are determined by the IC.



3.1.3 Bias assist

MS1003SH and MS1004SH incorporate an assist function to supply energy to VCC so that the voltage does not drop below ”Under-voltage lockout” (VCC (stop stby)) = 7 V(typ) or (VCC (stop normal)) = 8V(typ) to cause oscillation stop when it drops immediately after oscillation initiation at startup. This function eliminates the oscillation stop period at startup.

Shown below is a schematic diagram of VCC startup incorporating the bias assist function.



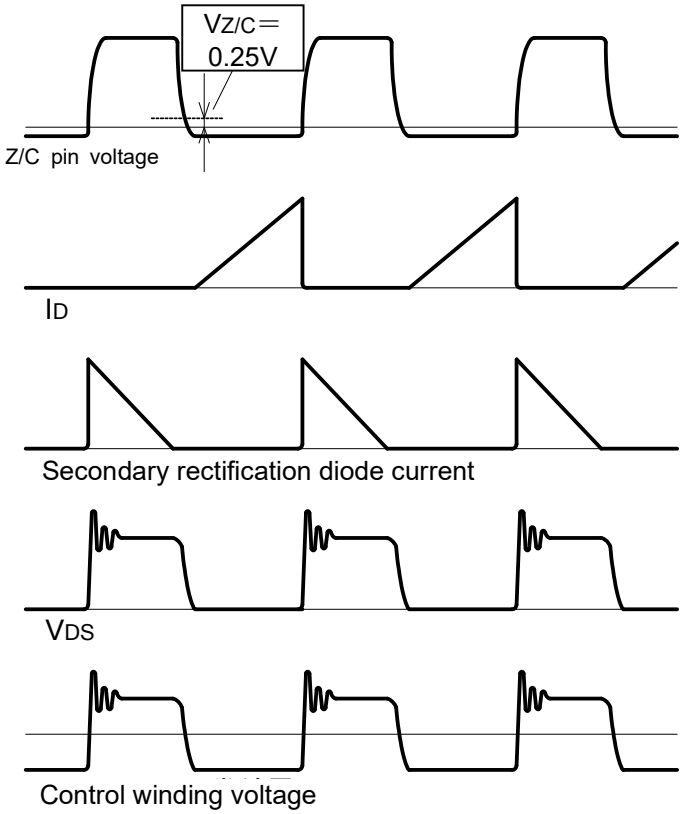
3.2 Oscillation

3.2.1 On-trigger circuit

As shown to the right, when a negative edge of Z/C pin voltage : $V_{Z/C}$ reaches "Zero current detection voltage" ($V_{Z/C}$) = 0.25 V (typ), the gate signal is output, and the main switching device is turned on.

Current-critical operations are performed by detecting energy discharge timing with the control winding voltage : V_{NC} before turning on the main switching device.

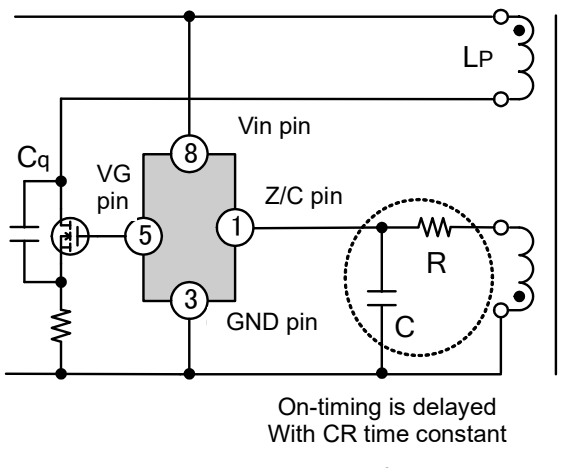
To minimize noise, negative edge detection detects a trigger while $V_{Z/C}$ falls from Hi to Low. The $V_{Z/C}$ = 0.25 V incorporates 50 mV hysteresis for improved noise resistance.

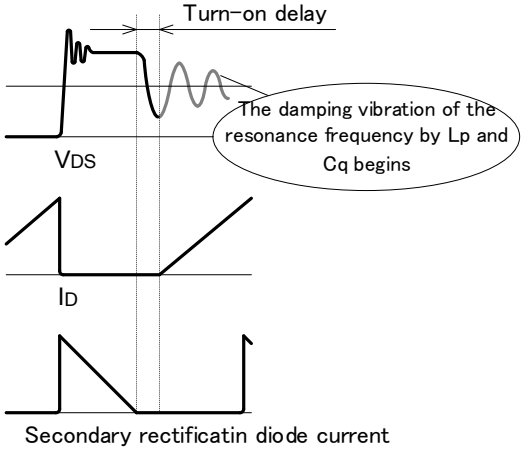


3.2.2 Quasi-resonance

In a circuit having resonating capacitor Cq between the drain and the source of the main switching device, as shown to the right, when the secondary diode current reaches 0 A, damping begins at the resonance frequency based on the primary inductance Lp of the main transformer and the resonating capacitor.

Adjusting the time constant of the CR connected to the Z/C pin as shown on the right allows the main switching device to be turned on at a bottom of the damping voltage waveform, thereby reducing turn-on losses.

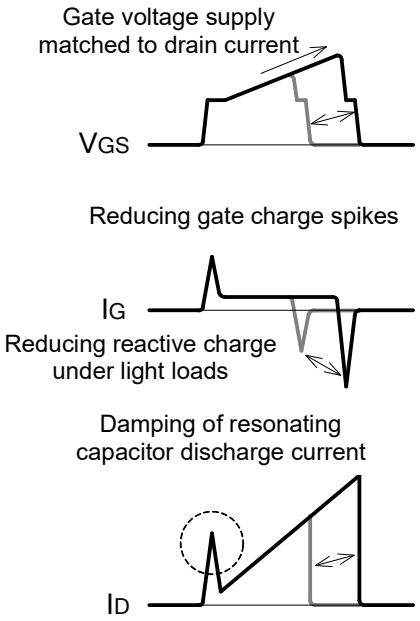




3.2.3 Soft drive

The soft drive circuit supplies a trigger voltage slightly greater than the gate threshold of the main switch as a gate drive voltage before constant voltage driving begins. After, this prevents the supply of greater gate voltage than necessary, because gate voltage supply matched to the drain current : ID.

The soft drive reduces losses by the gate charge voltage, reduces reactive charge under light loads and reduces noise by controlling the resonating capacitor discharge peak current.



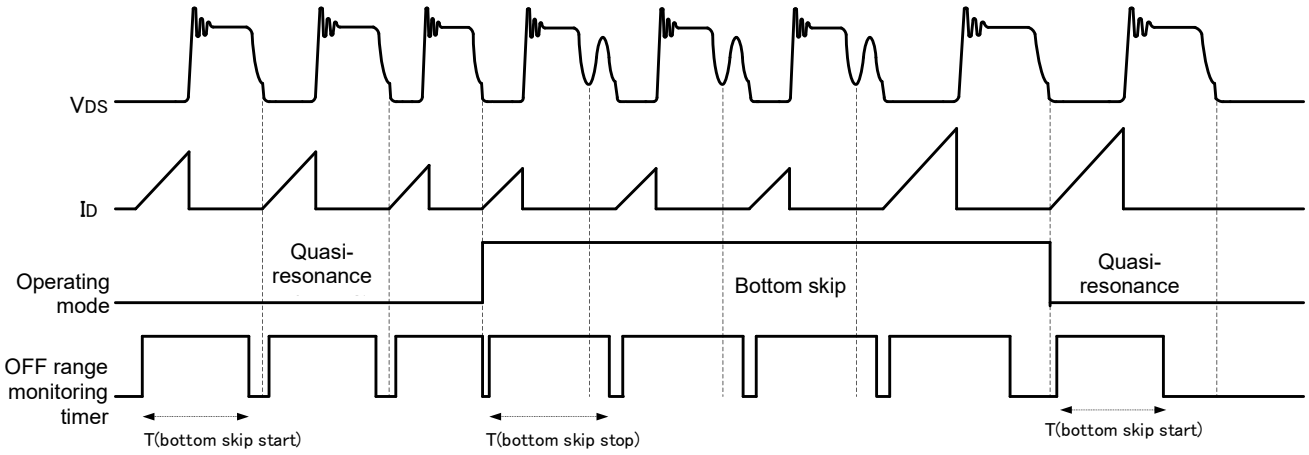
3.2.4 Bottom skip operation

The MS1003SH and MS1004SH monitor the switching cycle If the switching cycle length becomes shorter than “Bottom skip start time” (T (bottom skip start)) = 7.5 μs (typ), the IC enter the following modes:

MS1003SH moves from the normal quasi-resonance mode to the 1 bottom skip mode (Turn-on at the second bottom).

MS1004SH moves from the normal quasi-resonance mode to the 2 bottom skip mode (Turn-on at the second bottom).

In bottom skip mode, the MS1003SH extends the off-period by a cycle of resonance and the MS1004SH by two cycles of resonance. This controls an increase in the frequency. Once in bottom-skip mode, the off-time monitoring timer setting changes. When the time from turn-on to the first bottom becomes longer than “Bottom skip stop time” (T (bottom skip stop)) = 13 μs (typ), the IC returns to normal quasi-resonance mode. Using hysteresis in this manner prevents jitter and acoustic noise.



Sequence of MS1003SH

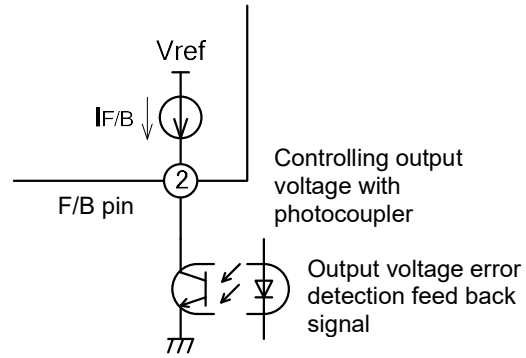
3.2.5 Output voltage control

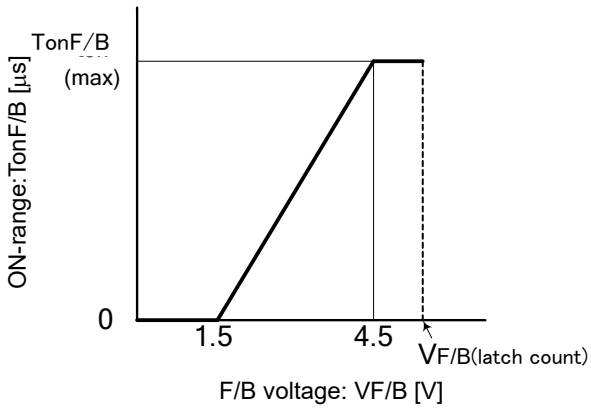
The MS1003SH and MS1004SH control the output voltage : Vo with the on-time (TonF/B) proportional to the F/B Vref voltage : $V_{F/B}$.

TonF/B becomes “F/B Minimum on time ” (TonF/B (min)) when VF/B is 1.5 V, and “F/B Maximum on tome ” (TonF/B Controlling output 2 (max)) when VF/B is 4.5 V

The F/B current : $I_{F/B}$ flows from the F/B pin. The Output voltage impedance of the photocoupler transistor externally error detection connected between the F/B pin and the GND pin is varied by feed back signal a control signal from the secondary output detection circuit, thereby controlling the on-time of the main switching device to produce a constant voltage.

“Timer latch count start voltage ” (VF/B (latch count)) = 4.6 V (typ) is set up for the F/B pin. When the voltage exceeds the set level, the timer begins counting. After maintaining this state for approximately 2 s (T(latch count)), the IC is latched.





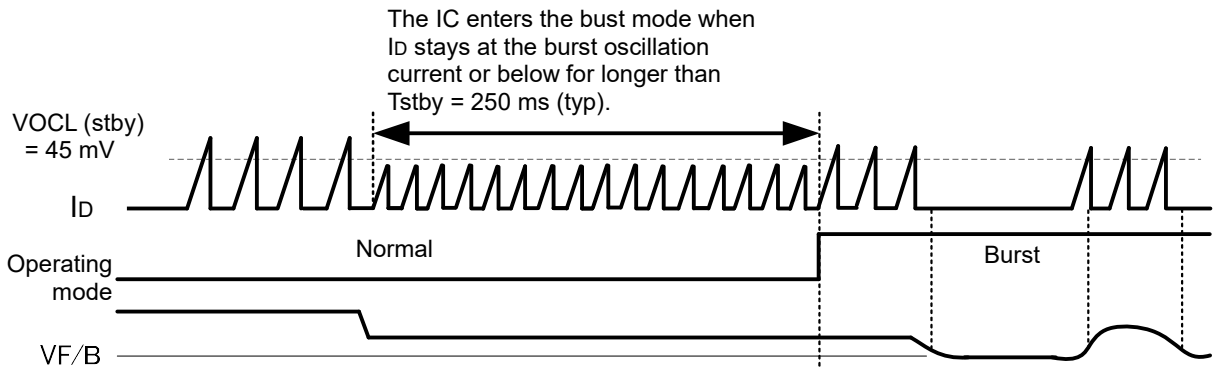
3.3 Burst mode oscillation

3.3.1 Auto-burst mode (Auto-Standby mode)

The MS1003SH and MS1004SH switch between normal mode and burst mode automatically (auto-burst). This enables low standby power consumption with no other components required for standby mode.

1) Switching from normal mode to burst mode

The IC switches from normal mode to burst mode when the load becomes lighter and the OCL pin detects I_D at ”Standby switch voltage ” (VOCL (stby)) = 45 mV (typ) or less for longer than “Standby switch time ” (Tstby) = 250 ms (typ).



2) Burst mode control

In burst mode, the OCL pin detects ID, and every pulse is limited to “Standby threshold voltage” (VTH (stby)) = 60mV (typ) to control oscillation.

Vo is controlled linearly in normal mode. In burst mode, oscillation begins when the VF/B reaches “On-State voltage” (VF/B (stby start)) = 1.8 V (typ) and stops when VF/B falls to “Under-Voltage lockou” (VF/B (stby stop)) = 0.8 V (typ). This control causes voltage ripples and intermittent oscillation, reducing switching loss per unit time and thereby reducing standby power consumption.

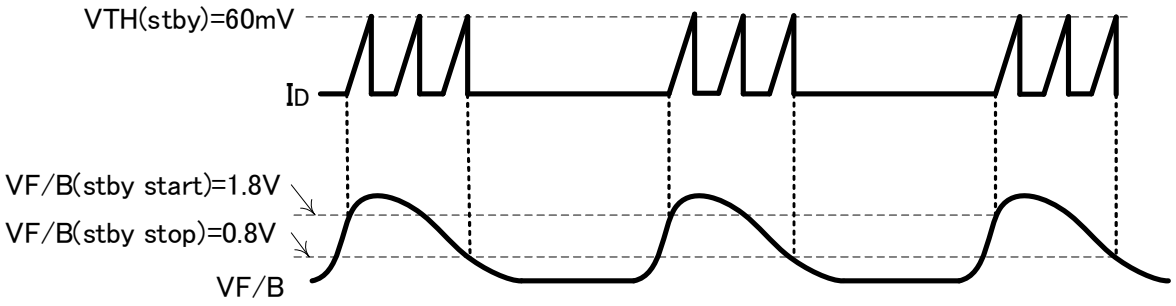
The following thresholds of VCC also change from normal mode:

◆“Under-Voltage lockout” and “Start-Up circuit on voltage” are lowered by 1V from normal mode.

“Under-Voltage lockout” : VCC (stop normal) = 8 V (typ) → VCC (stop stby) = 7 V (typ)

“Start-Up circuit on voltage” : VCC(stup on normal) = 9 V (typ) → VCC(stup on stby) = 8 V (typ)

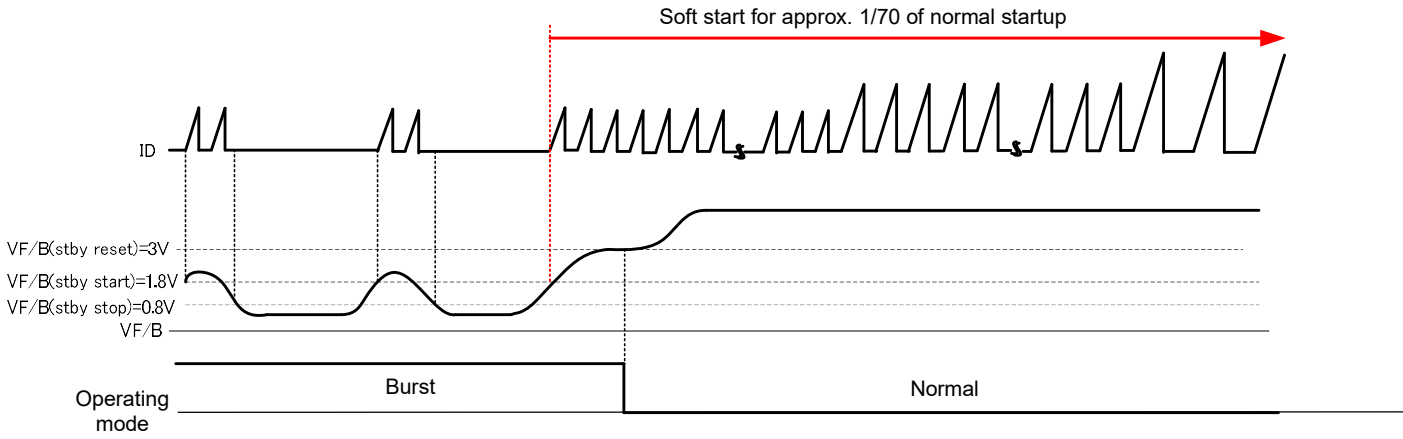
These allow down to the VCC setting in burst mode and further reduce power consumption.



3) Switching from burst mode to normal mode

The IC switches automatically to normal mode when the load becomes heavier and the VF/B voltage rises and exceeds VF/B (stby reset) = 3 V (TYP).

The thresholds changed at standby return to previous levels when the IC returns from burst mode to normal mode. At the same time, soft start activates for approximately 1/70 of the normal startup to prevent jitter and other problems during mode switching.



3.3.2 Super standby mode

Super-standby mode is an intermittent oscillation mode that minimizes power losses under micro loads. The function helps reduce input power.

1) Switching from normal mode or auto burst mode to super standby mode

The IC switches from normal mode or auto-burst mode to super-standby mode by stopping the external clamp of VZ/C using a signal and by applying “SP Standby switch Z/C voltage” (VZ/C (sp stby)) = 3 V (typ) or more per cycle.

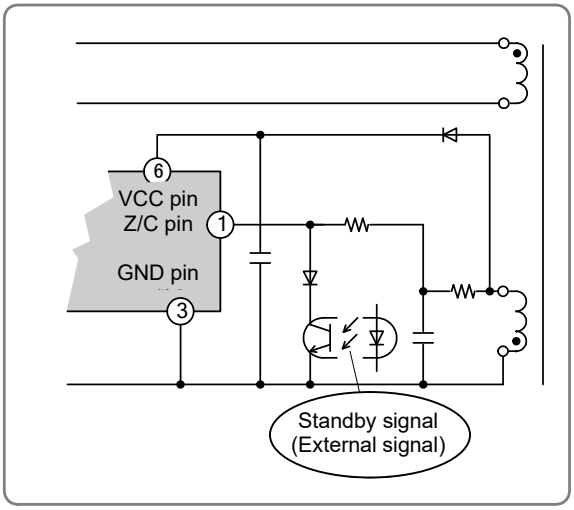
In super-standby mode, the IC promptly lowers VCC pin VCC to “SP Standby On-state voltage” (VCC (sp 1 stby start)) = 8.7 V (typ) to shift seamlessly from Z/C pin direct control to indirect control.

◆Standby signal ON (Photocoupler lights up):

VZ/C clamp ⇒ Normal mode or auto burst mode

◆Standby signal OFF (Photocoupler goes out):

VZ/C clamp released ⇒ Super standby mode



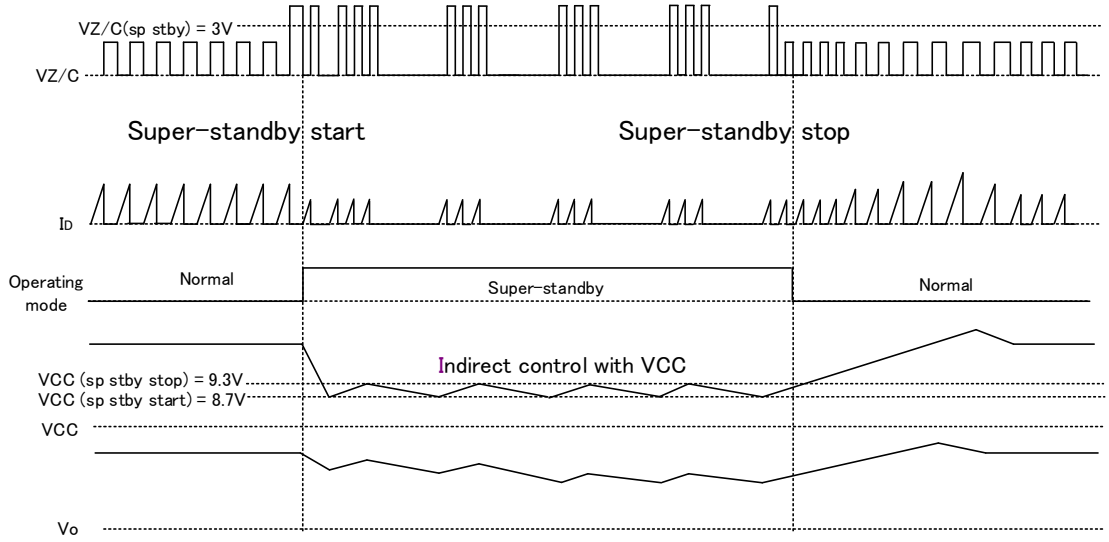
2) Super-standby control

In super-standby mode, control shifts from direct control using the F/B pin to indirect control using the VCC pin. Furthermore, On-State voltage and Under-voltage lockout are as follows.

super-standby On-State voltage: VCC (sp stby start) = 8.7 V (typ)

super-standby Under-voltage lockout: VCC (sp stby stop) = 9.3 V (typ)

Control is implemented with a lower voltage than VCC during normal operations. Vo is kept below regulation voltage, thereby bypassing activation of F/B pin photocoupler and reducing power consumption.



3) Switching from super-standby mode to normal mode or auto-burst mode

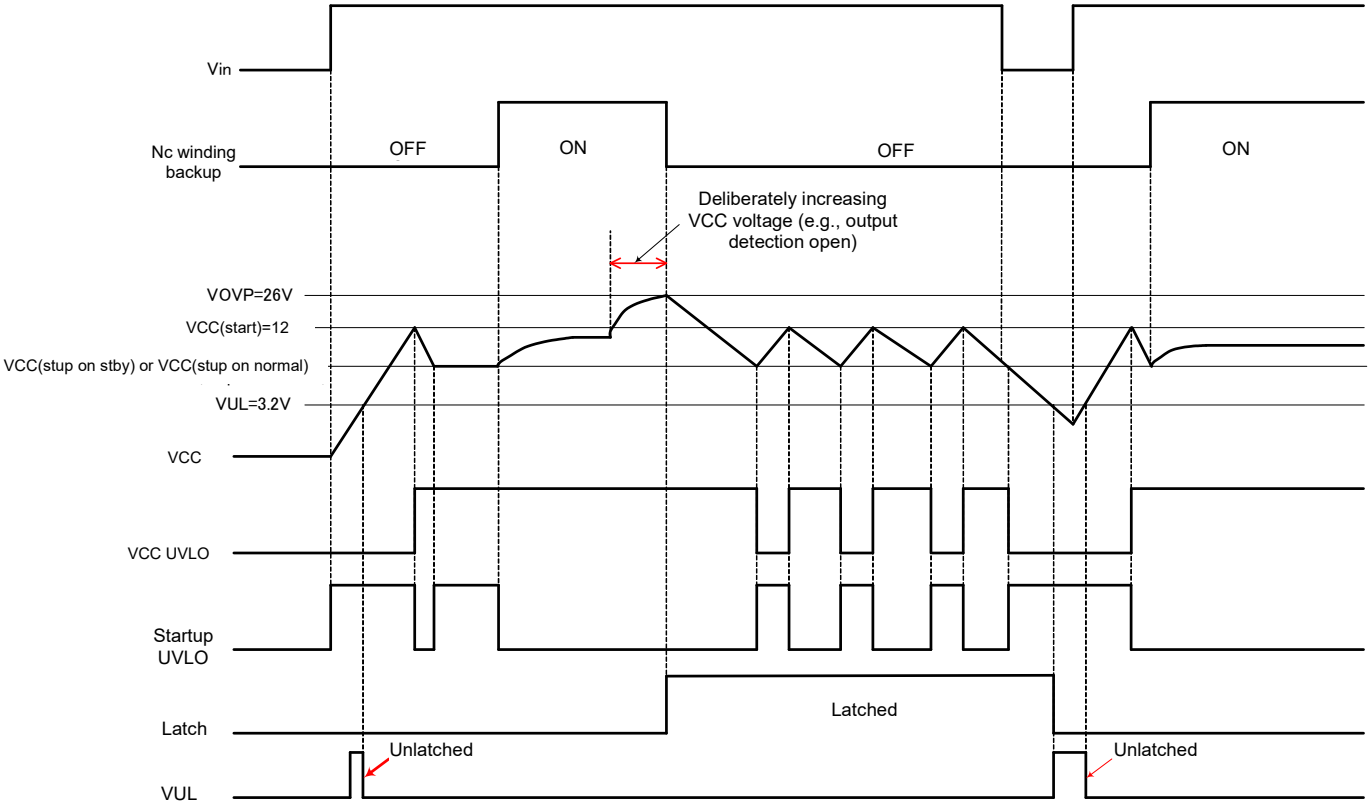
The IC exits super-standby mode by clamping VZ/C at 3 V or less using an external signal.

3.4 Protection functions

3.4.1 VCC overvoltage protection latch (OVP)

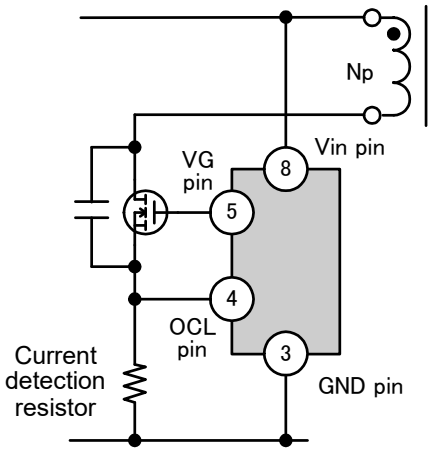
The MS1003SH and MS1004SH incorporate an overvoltage protection circuit (OVP).

The IC is latched when VNC exceeds “Over-Voltage threshold” (VOVP) = 26 V (typ) to provide indirect overvoltage protection for the secondary output (Vo). The IC is unlatched by momentarily dropping the VCC to “Latch circuit reset voltage” (VUL) = 3.2 V (typ) or below.

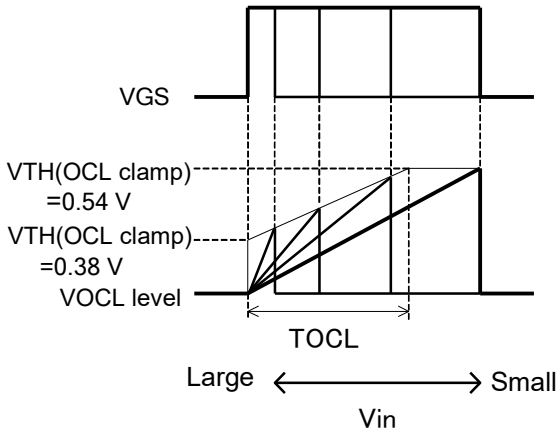


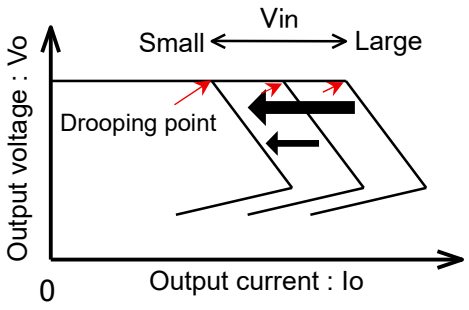
3.4.2 Overcurrent protection

A current detection resistor is connected between the OCL pin and the GND pin to detect the source current of the main switching device. The main switching device current is limited by pulse-by-pulse operation using a threshold voltage that varies with the on-time.



This current limit protection function incorporates a function to correct dependence on input voltage : Vin. The function changes the OCL threshold on the IC from the ” Over current limit correction start voltage” (VTH (OCL start)) = 0.38 V (typ) to “Over current limit correction clamp voltage” (VTH (OCL) clamp) = 0.54 V (typ) linearly with the on-time. Since the slope (di/dt) of I_D of the main switching device is proportional to Vin, when Vin increases, the current reaches the OCL threshold with smaller a main switching device peak current : I_{DP}, and the drooping-point is corrected

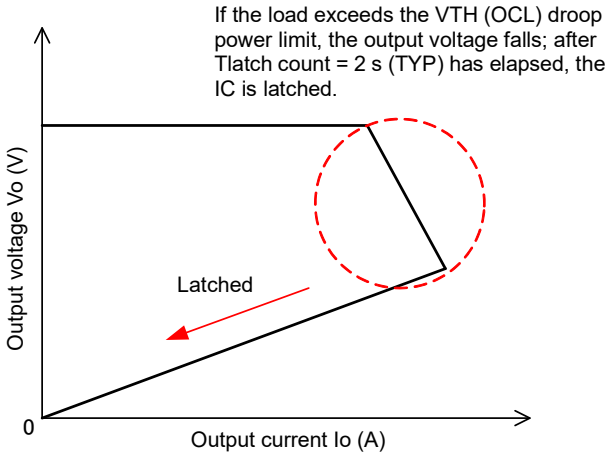




3.4.3 Overload protection (Timer latch circuit)

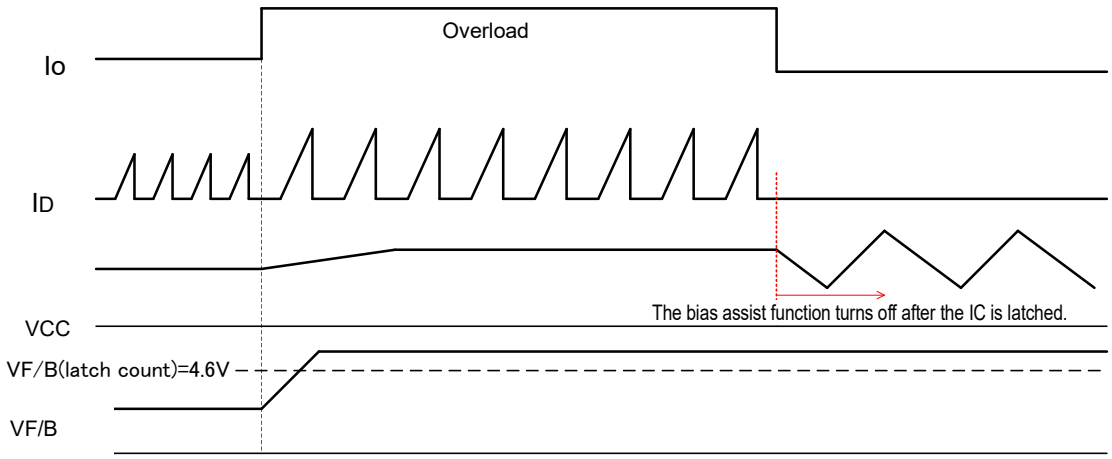
The overload timer latch function is a protection function that latches the IC when the VF/B stays at " Timer latch count start voltage " (VF/B (latch count)) = 4.6 V or more for more than "Timer latch count "(T(latch count)) = 2 s.

The power limit for protection is activated if power exceeds the power limit set as the overcurrent limit VTH (OCL), and the Vo begins to fall. VF/B increases beyond the control limit, and the VF/B increases to the VF/B (latch count) = 4.6 V or more. The timer detects this voltage and begins counting.



When the increase in voltage is detected continuously for T(latch count) = 2 s, the IC is latched to prevent a persisting overload. The timer is set for 2 seconds to avoid false detection.

The timer is reset if the VF/B drops below the VF/B (latch count) = 4.6 V or if the VCC drops below the VUL as the timer counts. After the IC is latched, the bias assist function of the startup circuit turns off to reduce heat buildup in the IC.



3.4.4 VCC-GND short circuit protection

If VCC and GND short-circuit, current flows continuously to the startup circuit, and heat builds up in the IC. A function reduces “VCC current” (ICC) in the event of short circuits to prevent excessive heat buildup.

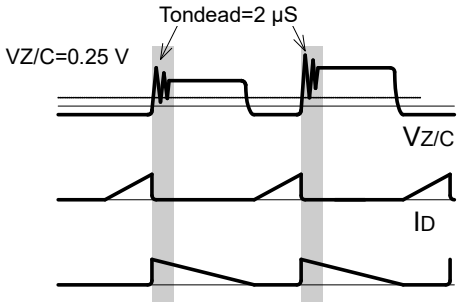
3.4.5 Leading edge blank (LEB)

The MS1003SH and MS1004SH incorporate “Leading edge blanking time” (TLEB) = 300 ns, which rejects trigger signals from ID detection circuit for a certain period of time after the main switching device is turned on to improve the noise margin.

This function prevents false detection due to a gate drive current generated the moment the main switching device is turned on or to a current discharged from the resonating capacitor.

3.4.6 On-trigger malfunction prevention circuit (Tondead)

At startup or in the event of a load short circuit, Vo drops to levels significantly below the set voltage. Since the control coil voltage is proportional to Vo, it drops significantly as well. In this case, a false on-trigger timing may be detected due to the ringing voltage while the device is off. The device may be turned on before the current critical point.



To address this problem, the MS1003SH and MS1004SH incorporate a circuit for preventing on-trigger malfunctions at startup or in the event of short circuits.

This function disables “On dead time” (Tondead) = 2 μs after the main switching device in the IC is turned off. This prevents false detection due to the ringing voltage while the device is off.

3.4.7 Thermal shutdown circuit (TSD)

The MS1003SH and MS1004SH incorporate a thermal shutdown circuit. The IC is latched at “Thermal shutdown temperature” 150°C (typ), and oscillation is stopped. The IC is unlatched by momentarily lower VCC to the VUL or below.

4. Pin functions

4.1 Z/C pin

The Z/C pin detects the NC winding voltage and outputs a turn-on signal. The pin has the following functions:

1) Gate on-trigger
2) Bottom-skip
3) Switching between super-standby mode and normal mode
4) Prevention of false turn-on (Tondead)

4.2 F/B pin

The F/B pin determines the on-time during constant voltage control. The pin has the following functions:

1) Determination of the on-time for the F/B pin voltage (gate off-trigger)
2) Timer latch protection during no control or power limit over

4.3 GND pin

The GND pin is used as the ground reference of the IC.

4.4 OCL pin

The OCL pin uses a detection resistor to limit the primary current. The pin has the following functions:

1) Determination of the primary current peak during the four-step soft-start
2) Determination of the primary current peak during the auto-burst mode (auto-standby mode)
3) Determination of the maximum primary current peak (pulse-by-pulse)
4) Leading edge blank function

4.5 VG pin

The VG pin outputs a gate voltage and has the soft drive function:

1) Soft drive

4.6 VCC pin

The VCC pin is the IC power terminal and has the following functions:

1) UVLO
2) ON/OFF of the startup circuit
3) Bias assist function
4) Indirect control in super-standby mode
5) OVP latch
6) Unlatching
7) VCC-GND short circuit protection

4.7 Vin pin

The Vin pin is connected to the positive side of the input capacitor and is used to power on the IC.

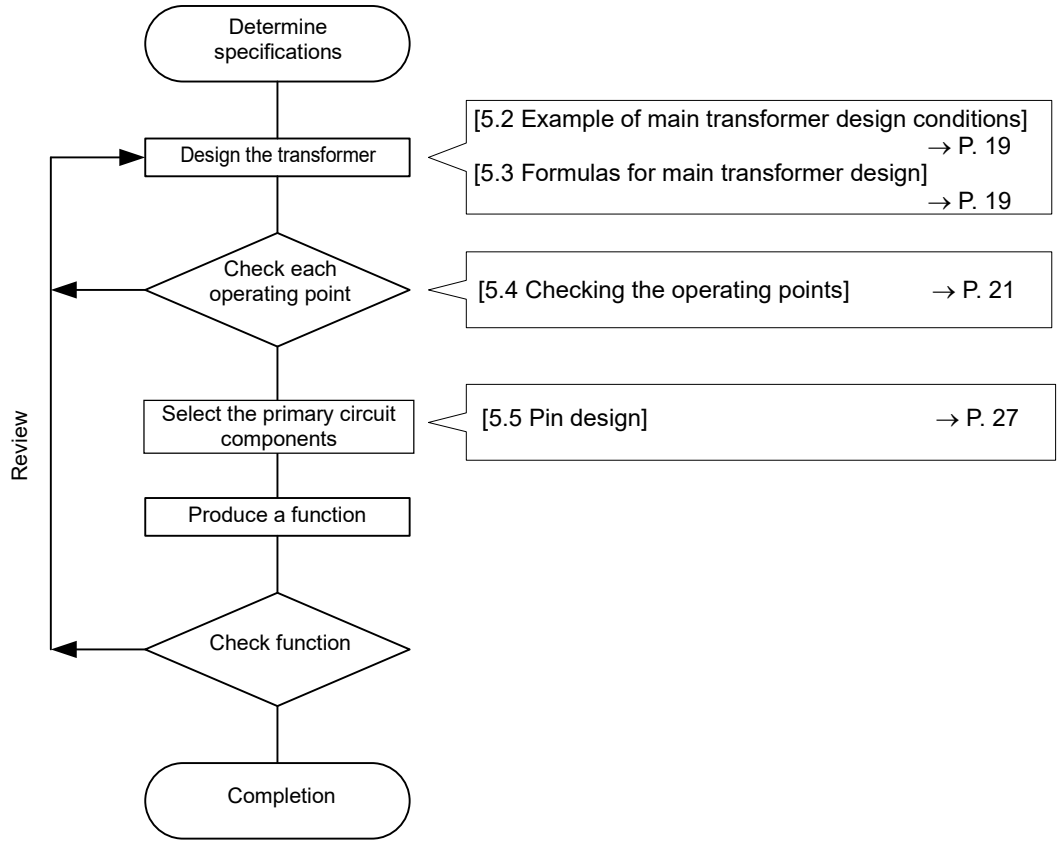
5. Design procedure

The design procedure presented in this section is intended to illustrate an example of electrical design procedure. Make sure insulation materials, insulation configuration, and structure meet the safety standards set forth by the relevant authorities. The following table shows the units for the parameters used in the formulas encountered in this section:

◆List of units used in the formulas in this section

Description	Unit	Description	Unit
Voltage	V (volt)	Time	s (second)
Current	A (ampere)	Length	mm (millimeter)
Power	W (watt)	Area	mm^2 (square millimeter)
Capacitance	F (farad)	Current density	A/mm^2 (ampere per square millimeter)
Inductance	H (henry)	Magnetic flux density	mT (millitesla)
Resistance	Ω (ohm)	Number of turns	turn

5.1 Design flow chart



5.2 Example of main transformer design conditions

The values below are provided as guideline values only. Make the appropriate adjustments to suit specific load conditions.

Description	Symbol	Reference value	Unit
Input voltage range	V_{AC}	85–276	[V]
Efficiency	η	0.80–0.85	-
Minimum oscillation frequency	$f_{(min)}$	35–50	[kHz]
On duty ratio	D	0.4–0.6	-
Capacity of resonating capacitor	Cq	100–3300	[pF]
Control coil voltage	V_{NC}	15–20	[V]
Magnetic flux density variation	ΔB	250–300	[mT]
Winding current density	α	4–6	[A/mm2]

◆ If the output capacity of the main switching device Coss is significant relative to the capacity setting of the resonating capacitor, Cq must be the capacity of the resonating capacitor plus Coss.

5.3 Formulas for main transformer design

1	Minimum DC input voltage	$V_{DC(\min)} = 1.2 \cdot V_{AC(\min)}$	[V]
2	Maximum DC input voltage	$V_{DC(\max)} = \sqrt{2} \cdot V_{AC(\max)}$	[V]
3	Maximum oscillation cycle	$T_{(\max)} = \frac{1}{f_{(\min)}}$	[s]
4	Maximum on-period	$t_{on(\max)1} = \frac{D}{f_{(\min)}}$	[s]
5	Maximum off-period	$t_{off(\max)} = \frac{N_{S1} \cdot V_{DC(\min)} \cdot t_{on(\max)1}}{Np \cdot (V_{O1} + V_{F1})} + tq$	[s]
6	Quasi-resonance-time	$tq = \pi \cdot \sqrt{Lp \cdot Cq}$	[s]
7	Maximum load power	$P_{O(\max)} = Vo \cdot I_{O(\max)}$	[W]
8	Maximum output power (reference value)	$P_L = 1.2 \cdot P_{O(\max)}$	[W]
9	Main switching device peak current	$I_{DP} = \frac{2 \cdot P_L}{\eta \cdot V_{DC(\min)} \cdot D}$	[A]

10	Primary winding inductance	$Lp = \frac{V_{DC(\min)} \cdot t_{on(\max)1}}{I_{DP}}$	[H]
11	Number of turns in primary winding	$Np = \frac{V_{DC(\min)} \cdot t_{on(\max)1} \cdot 10^9}{\Delta B \cdot Ae}$	[Turn]
12	Core gap	$\lg = \frac{4 \cdot \pi \cdot Ae \cdot Np^2 \cdot 10^{-10}}{Lp}$ ◆Ae: Effective sectional area of core [mm^2]	[mm]

◆The gap Ig must be the center gap value.

◆If the Ig is 1 mm or greater, review the transformer core size and oscillation frequency and consider a redesign.

13	Number of turns in control output winding	$N_{S1} = \frac{Np \cdot (V_{O1} + V_{F1}) \cdot (\frac{1}{f_{(\min)}} - t_{on(\max)1} - tq)}{V_{DC(\min)} \cdot t_{on(\max)1}}$	[Turn]
14	Number of turns in non-control output winding	$N_{S2} = N_{S1} \cdot \frac{V_{O2} + V_{F2}}{V_{O1} + V_{F1}}$	[Turn]
15	Number of turns in control winding	$Nc = N_{S1} \cdot \frac{V_{NC} + V_{FNC}}{V_{O1} + V_{F1}}$	[Turn]

◆Symbols used in formulas 13 to 15

Control output winding : Output voltage 1	V_{O1}	Output of control output winding : Rectification diode forward voltage	V_{F1}
Non-control output winding : Output voltage 2	V_{O2}	Output of non-control output winding : Rectification diode forward voltage	V_{F2}
Control winding : Output voltage 1	V_{NC}	Output of control winding : Rectification diode forward voltage	V_{FNC}

◆ If the control winding voltage V_{NC} is not well regulated, set a lower value. To make the most of the super standby function, set the voltage higher.

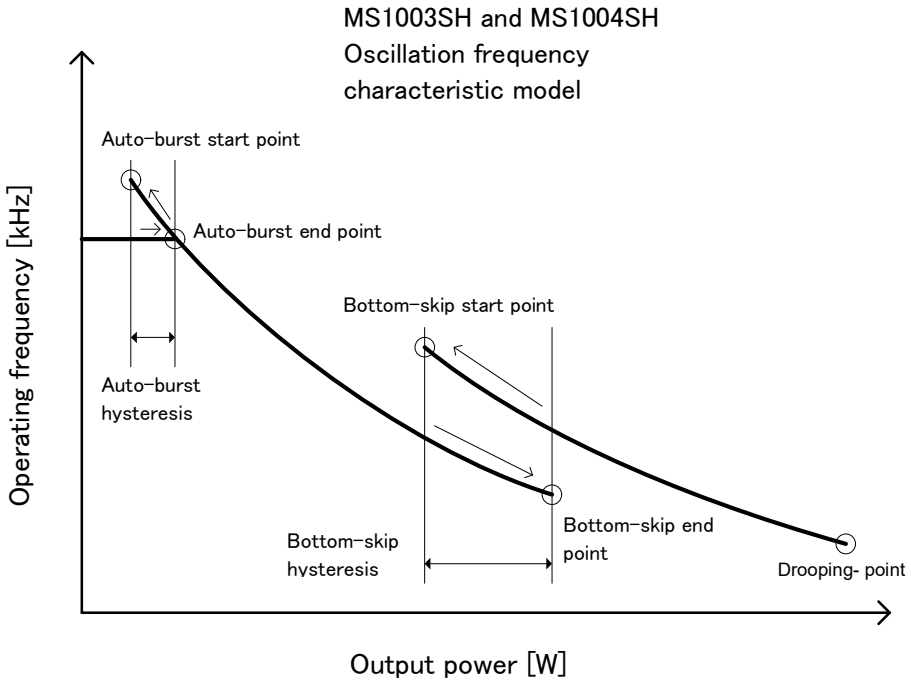
16	Primary winding sectional area	$A_{NP} = \frac{2 \cdot \sqrt{D} \cdot Po}{\alpha \cdot \sqrt{3} \cdot \eta \cdot V_{DC(\min)} \cdot t_{on(\max)1} \cdot f_{(\min)}}$	[mm^2]
17	Secondary winding sectional area	$A_{NS} = \frac{2 \cdot Io \cdot \sqrt{1 - D - (tq \cdot f_{(\min)})}}{\alpha \cdot \sqrt{3} \cdot (t_{off(\max)} - tq) \cdot f_{(\min)}}$	[mm^2]

◆Shindengen recommend a wire diameter of 0.2mm or greater for the Nc winding to simplify calculations.

5.4 Checking the operating points

The MS1003SH and MS1004SH have points of change at which the oscillation frequency changes according to the functions of the control IC.

Identifying each point helps predict the behavior of a prototype power supply. The following chart shows a model of operating frequency characteristics relative to output power. Knowing each operating point will provide approximate levels of the power, hysteresis width and droop point at these points of change.



The operating points to be calculated in this section are circled on the chart above.

◆Bottom-skip start and end points

◆Auto-burst start and end points

◆Drooping-point

Obtain these points to check the following:

Is the standby operation properly performed in standby mode?

Is the bottom-skip hysteresis sufficient?

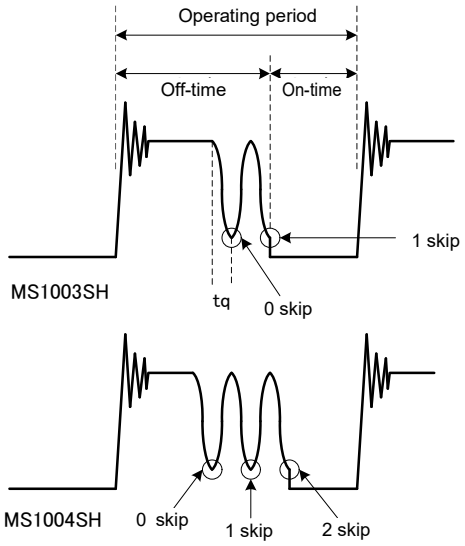
Is the drooping-point sufficiently greater than the output?

5.4.1 Variables in formulas

Description	Symbol	Unit
DC input voltage setting	V_{DC}	[V]
On-time under each condition	ton	[s]
Off-time under each condition	toff	[s]
Main switching device peak current under each condition	I_{DP}	[A]
Output power under each condition	Po	[W]
Primary current detection resistance	R(ocl)	[Ω]
OCL pin auto-burst threshold voltage	Vburst	[V]
OCL pin current detection threshold voltage	Vth(ocl)	[V]

The diagram to the right shows oscillation waveform models, including numbers of bottoms to skip and tq.

For other symbols, see Section 5.3 and the specification.



Switching waveform model

5.4.2 Bottom-skip start power

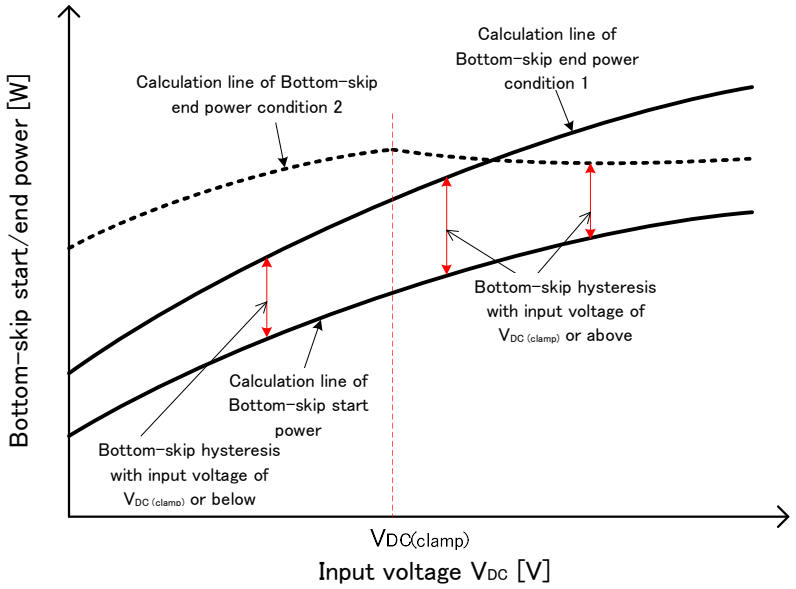
18	On-time	$ton = \frac{Np \cdot (T_{(\text{bottom\_skip\_start})} - tq) \cdot (V_{O1} + V_{F1})}{N_{S1} \cdot V_{DC} + Np \cdot (V_{O1} + V_{F1})}$	[s]
19	Off-time	$toff = T_{(\text{bottom\_skip\_start})} - ton$	[s]
20	Main switching device peak current	$I_{DP} = \frac{V_{DC} \cdot ton}{Lp}$	[A]
21	Bottom-skip start power	$Po = \frac{{V_{DC}}^2 \cdot ton^2 \cdot \eta}{2 \cdot Lp \cdot T_{(\text{bottom\_skip\_start})}}$	[W]

If the bottom-skip start power obtained by the formulas above is greater than the bottom-skip end power obtained in Section 5.4.3, the hysteresis is insufficient; redesign the transformer.

5.4.3 Bottom-skip end power

The bottom-skip function ends when either Condition 1 or Condition 2 is met. The bottom-skip end power will be the “bottom-skip end power 1 of the formula 25 of Condition 1” or the “bottom-skip end power 2 of the formula 30 or the bottom-skip end power 3 of the formula 34 of Condition 2,” whichever is smaller. (Depending on the input voltage you want to calculate, compare either the bottom-skip end power 2 or 3 of Condition 2 to bottom-skip end power 1.)

The chart on the next page shows model curves of bottom-skip start and end power levels relative to input voltage.



[Condition 1] The operating frequency fulfills T (bottom_skip_stop).

◆In place of coefficient "A" in the formulas, substitute 1 for the MS1003SH and 2 for the MS1004SH.

22	On-time	$ton = \frac{Np \cdot (T_{(\text{bottom\_skip\_stop})} - tq) \cdot (V_{O1} + V_{F1})}{N_{S1} \cdot V_{DC} + Np \cdot (V_{O1} + V_{F1})}$	[s]
23	Off-time	$toff = T_{(\text{bottom\_skip\_stop})} + 2A \cdot tq - ton$	[s]
24	Main switching device peak current	$I_{DP} = \frac{V_{DC} \cdot ton}{Lp}$	[A]
25	Bottom-skip end power 1	$Po = \frac{{V_{DC}}^2 \cdot ton^2 \cdot \eta}{2Lp \cdot (T_{(\text{bottom\_skip\_stop})} + 2A \cdot tq)}$	[W]

[Condition 2] The OCL pin voltage reaches the current detection threshold voltage in bottom-skip mode.

Under this condition, Vth (ocl) varies with input voltage. First, calculate the input voltage : $V_{DC\ (clamp)}$ at the point of change in Vth (ocl). If V_{DC} does not exceed $V_{DC\ (clamp)}$, apply the formulas in next page 1). If V_{DC} exceeds $V_{DC\ (clamp)}$, apply the formulas in next page 2).

The $V_{DC\ (clamp)}$ (Input voltage at the point of change in Vth (ocl)) is obtained with the following formula.

26	Input voltage at the point of change in Vth (ocl)	$V_{DC(clamp)} = \frac{Lp \cdot Vth_{(OCL)clamp}}{TOCL \cdot R_{(OCL)}}$	[V]

1) $V_{DC} < V_{DC\ (clamp)}$

◆In place of the coefficient "A" in the formulas, substitute 1 for the MS1003SH and 2 for the MS1004SH.

27	On-time	$ton = \frac{Lp \cdot Vth_{(OCL)clamp}}{V_{DC} \cdot R_{(OCL)}}$	[s]
28	Off-time	$toff = \frac{V_{DC} \cdot N_{S1} \cdot ton}{Np \cdot (V_{O1} + V_{F1})} + (2A+1) \cdot tq$	[s]
29	Main switching device peak current	$I_{DP} = \frac{Vth_{(OCL)clamp}}{R_{(OCL)}}$	[A]
30	Bottom-skip end power 2	$Po = \frac{V_{DC} \cdot Vth_{(OCL)clamp} \cdot \eta \cdot ton}{2 \cdot R_{(OCL)} \cdot (ton + toff)}$	[W]

2) $V_{DC} > V_{DC\ (clamp)}$

◆In place of the coefficient "A" in the formulas, substitute 1 for the MS1003SH and 2 for the MS1004SH.

31	On-time	$ton = \frac{Vth_{(OCLstart)}}{\frac{V_{DC} \cdot R_{(OCL)}}{Lp} - \frac{(Vth_{(OCL)clamp} - Vth_{(OCLstart)})}{T_{(ocl)}}}$	[s]
32	Off-time	$toff = \frac{V_{DC} \cdot N_{S1} \cdot ton}{Np \cdot (V_{O1} + V_{F1})} + (2A+1) \cdot tq$	[s]
33	Main switching device peak current	$I_{DP} = \frac{V_{DC} \cdot ton}{Lp}$	[A]
34	Bottom-skip end power 3	$Po = \frac{V_{DC}{}^2 \cdot ton^2 \cdot \eta}{2 \cdot Lp \cdot (ton + toff)}$	[W]

5.4.4 Auto-burst start/end power

For Vburst in the formulas, substitute the VOCL (stby) or VTH (stby) indicated under "Auto standby modde" of "Electric/thermal characteristics" in the specification.

To obtain the auto-burst start power, substitute VOCL (stby) = 0.045 V in place of Vburst.

To obtain the auto-burst end power, substitute VTH (stby) = 0.060 V in place of Vburst.

◆In place of the coefficient "A" in the formulas, substitute 1 for the MS1003SH and 2 for the MS1004SH.

35	On-time	$ton = \frac{Lp \cdot Vburst}{V_{DC} \cdot R_{(OCL)}}$	[s]
36	Off-time	$toff = \frac{V_{DC} \cdot N_{S1} \cdot ton}{Np \cdot (V_{O1} + V_{F1})} + (2A+1) \cdot tq$	[s]
37	Main switching device peak current	$I_{DP} = \frac{Vburst}{R_{(OCL)}}$	[A]
38	Auto-burst start/end power	$Po = \frac{V_{DC} \cdot Vburst \cdot \eta \cdot ton}{2 \cdot R_{(OCL)} \cdot (ton + toff)}$	[W]

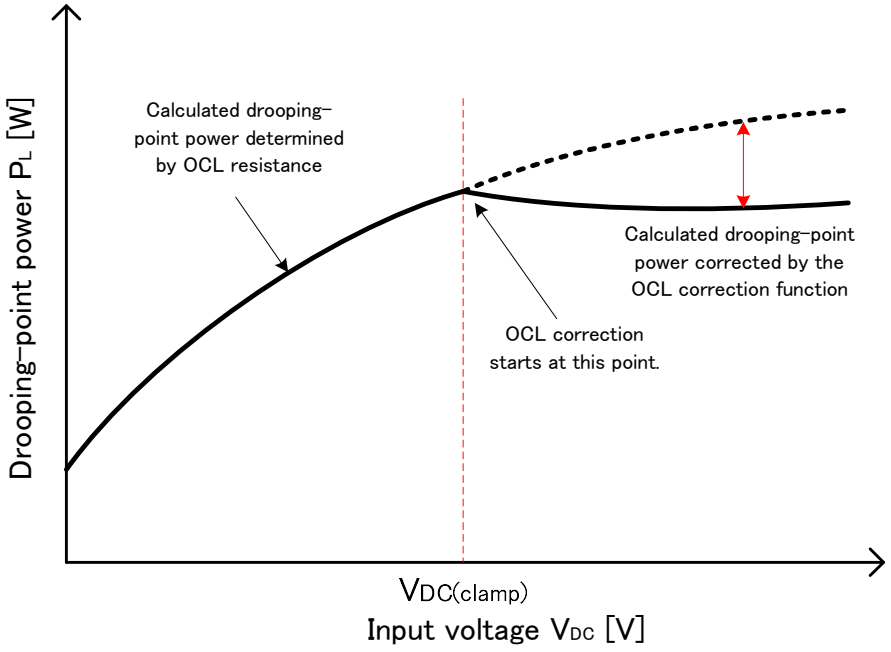
5.4.5 Drooping-point power

Vth (ocl) varies with input voltage. First, calculate the input voltage $V_{DC\ (clamp)}$ at the point of change in Vth (ocl). If VDC does not exceed $V_{DC\ (clamp)}$, apply the formulas in next page 1). If V_{DC} exceeds $V_{DC\ (clamp)}$, apply the formulas in next page 2).

Just as in Section 5.4.3, use the following formula to obtain the input voltage at the point of change in Vth (ocl).

26	Input voltage at the point of change in Vth (ocl)	$V_{DC(clamp)} = \frac{Lp \cdot Vth_{(OCL)clamp}}{TOCL \cdot R_{(OCL)}}$	[V]

The chart below shows a model curve of the relationship between input voltage and drooping-point power.



1) $V_{DC} < V_{DC\ (clamp)}$

39	On-time	$ton = \frac{Lp \cdot Vth_{(OCL)clamp}}{V_{DC} \cdot R_{(OCL)}}$	[s]
40	Off-time	$toff = \frac{V_{DC} \cdot N_{S1} \cdot ton}{Np(V_{O1} + V_{F1})} + tq$	[s]
41	Main switching device peak current	$I_{DP} = \frac{Vth_{(OCL)clamp}}{R_{(OCL)}}$	[A]
42	Drooping-point power	$P_L = \frac{{V_{DC}}^2 \cdot ton^2 \cdot \eta}{2 \cdot Lp \cdot (ton + toff)}$	[W]

2) $V_{DC} > V_{DC\ (clamp)}$

43	On-time	$ton = \frac{Vth_{(OCLstart)}}{\frac{V_{DC} \cdot R_{(OCL)}}{Lp} - \frac{(Vth_{(OCL)clamp} - Vth_{(OCLstart)})}{TOCL}}$	[s]
44	Off-time	$toff = \frac{V_{DC} \cdot N_{S1} \cdot ton}{Np \cdot (V_{O1} + V_{F1})} + tq$	[s]
45	Main switching device peak current	$I_{DP} = \frac{V_{DC} \cdot ton}{Lp}$	[A]
46	Drooping-point power	$P_L = \frac{{V_{DC}}^2 \cdot ton^2 \cdot \eta}{2 \cdot Lp \cdot (ton + toff)}$	[W]
47	Vth (ocl) at drooping-point	$Vth_{(ocl)} = \frac{(Vth_{(OCL)clamp} - Vth_{(OCLstart)})}{TOCL} \cdot ton + Vth_{(OCLstart)}$	[V]

The results of calculations for the operating points above are provided as guidelines. They may differ from actual power supply characteristics for various reasons, including power supply efficiency, filter circuit, and control IC signal delays.

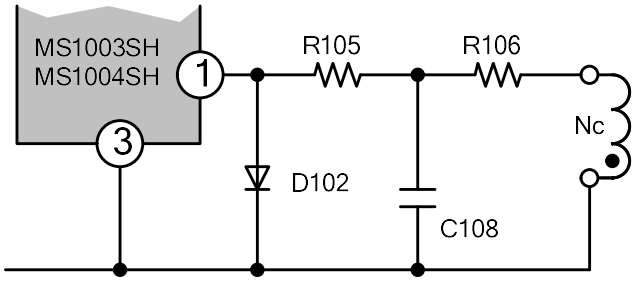
5.5 Pin design

5.5.1 Z/C pin (Pin 1)

The operating mode switching circuit described in this section incorporates a photocoupler that receives signals from the secondary side. For the secondary circuit configuration, see 6. Example circuit diagram.

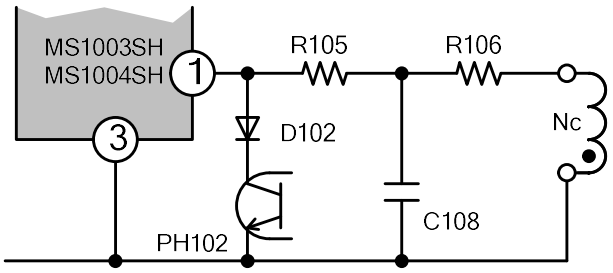
(1) Basic circuit

This is the simplest circuit configuration for designs requiring only normal mode. Since auto-burst mode is available, it is the easiest design for a power supply featuring standby mode.



(2) Circuit for using super standby mode

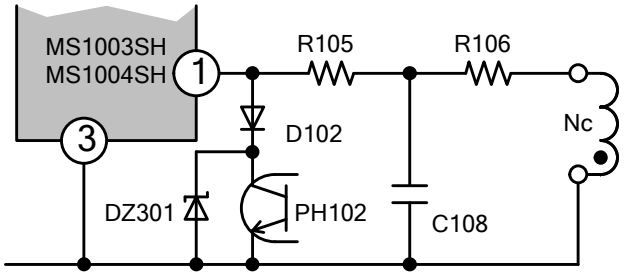
The diagram to the right shows the basic circuit for using super-standby mode. A photocoupler is added to switch the Z/C pin between high and low levels. If the photocoupler activates, the circuit operates in normal mode. If the photocoupler deactivates, the circuit operates in super standby mode.



The photocoupler current must be carefully set so that the Z/C pin voltage falls sufficiently low.

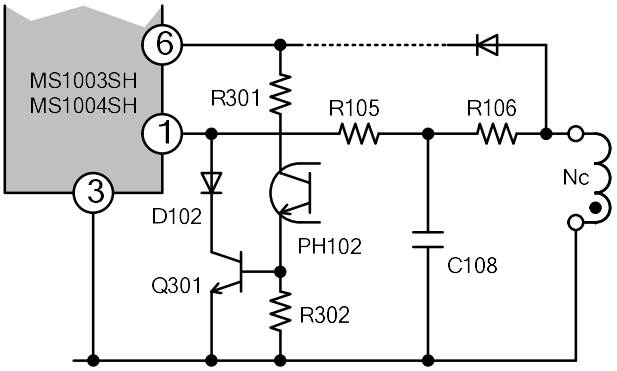
◆Protection for this circuit configuration

Protect with a zener diode (DZ301) if the insulation appears likely to break down between the photocoupler (PH102) and the primary or secondary side, as shown to the right.



(3) Circuit for operating the photocoupler at low current

This circuit uses less power to operate the PH102 in auto-burst mode, thereby slightly enhancing efficiency in auto-burst mode compared to circuit (2).

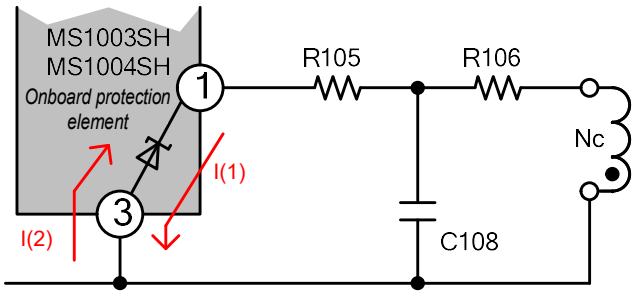


(4) Setting components

1) R105 + R106

The absolute maximum rating of the Z/C pin is ±5 mA. A zener diode is mounted for protection between the Z/C pin (Pin 1) and the GND pin (Pin 3). This diode determines the absolute maximum current rating. Set resistance so that the current does not exceed this level.

The diagram to the right shows a model circuit, which is a basic circuit with an onboard protection element (zener diode) added. I(1) and I(2) represent currents flowing to this onboard protection element. The current I(1) flows when the Nc winding output is a positive voltage. I(2) flows when the Nc winding output is a negative voltage.



I(1) and I(2) must not exceed the absolute maximum rating. In ordinary designs, set resistance so that these currents do not exceed 80% of the absolute maximum rating (± 4 mA).

The following table gives formulas for calculating the resistance R105 + R106:

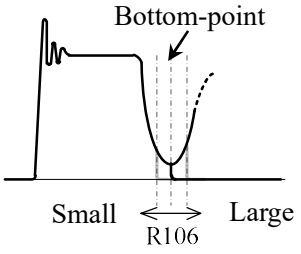
48	Resistance assuming a positive voltage for Nc winding	$R105 + R106 \geq \dfrac{\dfrac{Nc \cdot (V_{O1} + V_{F1})}{N_{S1}} - VCL(H)}{I_{①}}$	[Ω]
49	Resistance assuming a negative voltage for Nc winding	$R105 + R106 \geq \dfrac{\dfrac{Nc \cdot V_{DC(\max)}}{Np} - VCL(L)}{-I_{②}}$	[Ω]

VCL(H) and VCL(L) are the clamping voltages of the onboard protection element, a protective zener diode. The specification gives these values.

If the basic circuit configuration shown in Section (1) is used, I(1) flows to the D102. In this case, formula 48 may be disregarded.

2) R106 and C108

These components set up the quasi-resonance period tq. Adjust to the quasi-resonance bottom-point while monitoring actual waveforms.



Symbol	Initial design value
C108	100 pF
R106	1 kΩ or greater

The maximum voltage applied to both ends of C108 is calculated as shown in the formula 50.

Determine the withstand voltage of C108 by referring to the calculated value.

50	Maximum voltage applied to both ends of C108	$V_{C108} = (V_{O1} + V_{F1}) \dfrac{Nc}{N_{S1}} + V_{DC(max)} \dfrac{Nc}{Np}$	[V]

3) D102

This diode sets the Z/C pin to low to activate normal mode.

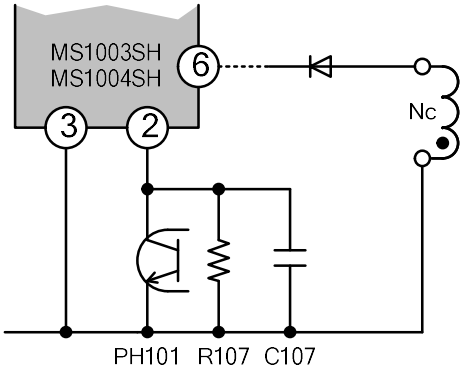
As described in section 3.2.1, the on-trigger circuit detects the Z/C pin voltage when it reaches VZ/C = 0.25 V (typ). Thus, the diode should not reduce the voltage below VZ/C. Make sure the diode has adequate VF to secure VZ/C. Also, select high-speed diodes (FRD) with a short reverse recovery time (trr).

5.5.2 F/B pin (Pin 2)

(1) Basic circuit

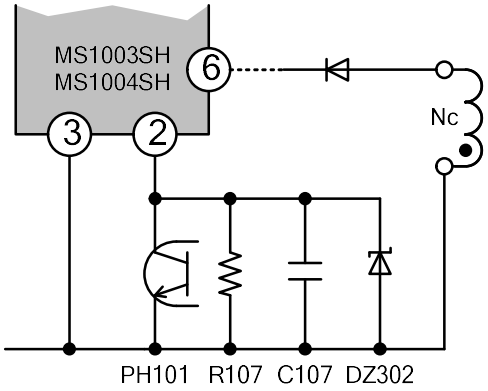
The diagram to the right shows the basic circuit. PH101 is a photocoupler for constant voltage control. R107 and C107 are noise reduction components.

C107 has a capacitance between 470 pF and 2200 pF. Set the initial design value to 1000 pF. R107 is set between 39 kΩ and 47 kΩ. Normally, it should be set to 47 kΩ. If the resistance falls below 39 kΩ, the timer latch function may be disabled.



(2) Circuit Protection

PH101 may exhibit insulation breakdown during a short circuit test. If so, protect the circuit using a zener diode, as shown to the right. A zener diode (DZ302) for 10 V or greater should have negligible effect on IC functions for normal use.

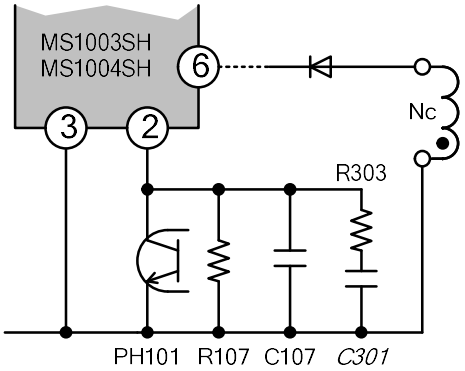


(3) Phase compensation of F/B pin

C107 is used not just to reduce noise, but to adjust feedback response. However, in a large-capacity or multi-output power supply, phase compensation by the secondary control circuit may be inadequate.

If so, add a circuit between the F/B pin and the GND pin, as shown to the right. Doing so can resolve various issues, including hunting.

Refer to the following table to determine constants.



	Initial design value
R303	4.7 kΩ
C301	0.1 μF

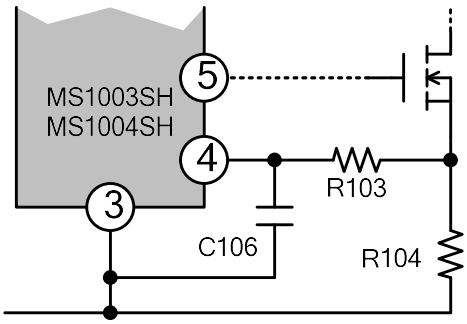
(4) Additional circuit to F/B pin

When adding a circuit to the power supply circuit due to load setting conditions or for other reasons, be careful to avoid disabling the timer latch function. Disabling the timer latch will affect power supply performance.

5.5.3 OCL pin (pin 4)

(1) Basic circuit

The diagram to the right shows the basic circuit.



The circuit consists of R104 for primary current detection and a filter circuit comprising R103 and C106.

R104: Resistance required in section 5.4

C106: Initial design value of 220 pF
Design values from 220 pF to 3300 pF

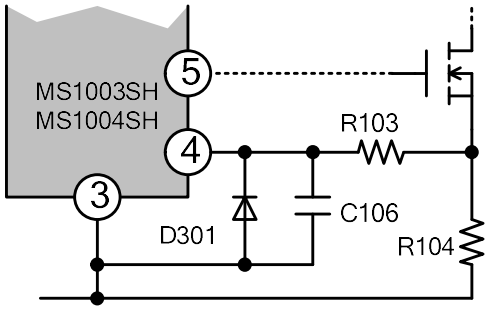
R103: Initial design value of 100 Ω
Design values from 100 to 470 Ω

Increase the constants if switching noise is significant and may lead to malfunctions.

(2) Protection for large output power

If oscillation noise is significant for instance, because output power is large a high negative voltage may be applied to the OCL pin. Since the MS series are single power supply ICs, a negative voltage may damage the IC or cause malfunctions.

The following diagram shows a circuit that incorporates a feature to protect the OCL pin against negative voltages. The added diode D301 should have small V_F (A Schottky barrier diode with a VF of 0.7V or less is recommended.) and should be connected as close as possible to the pin.

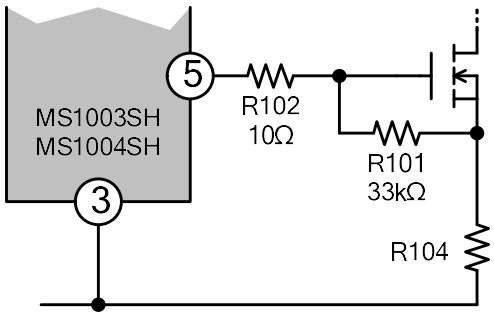


5.5.4 VG pin (Pin5)

(1) Basic circuit

The VG pin outputs switching signals. It can be used when the main switching device is a voltage-driven element.

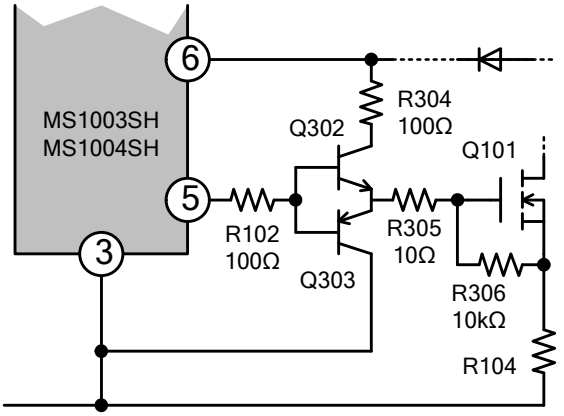
The diagram to the right shows the basic circuit configuration. The initial design values should be 10 Ω for the gate resistor R102 and 33 kΩ for the resistor R101 between the gate and the source.



(2) Circuit requiring a drive circuit

The main switching device driving performance of the MS series is specified under “Soft drive” of “Electric/thermal characteristics” in the specification. A circuit for enhancing the driving performance is required between the VG pin and the main switching device as shown to the right if the main switching device cannot be driven directly by the VG pin in the basic circuit (1).

Refer to the diagram to the right to determine constants.



◆Use the gate total charge quantity Qg of the main switching device as a guide for determining whether a driving circuit is required.

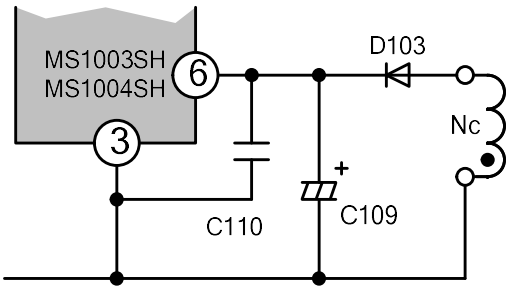
Qg of main switching device < 21 nC	No driving circuit required
Qg of main switching device > 21 nC to 25 nC	Driving circuit required

5.5.5 VCC pin

(1) Basic circuit

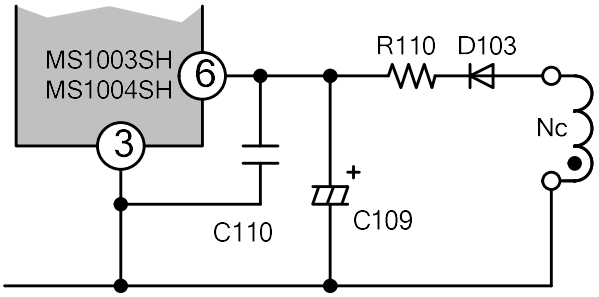
The diagram to the right is the basic circuit. The circuit consists of D103 and C109 for rectifying the Nc winding output and C110 for noise reduction between VCC and GND.

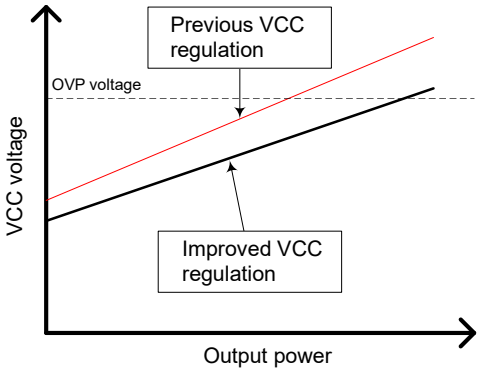
The D103 selects a fast diode (FRD) with a short reverse recovery time (trr). The C110 is selected at around 0.22 µF using a capacitor with good frequency characteristics.



(2) Measure ① for Poor VCC voltage regulation

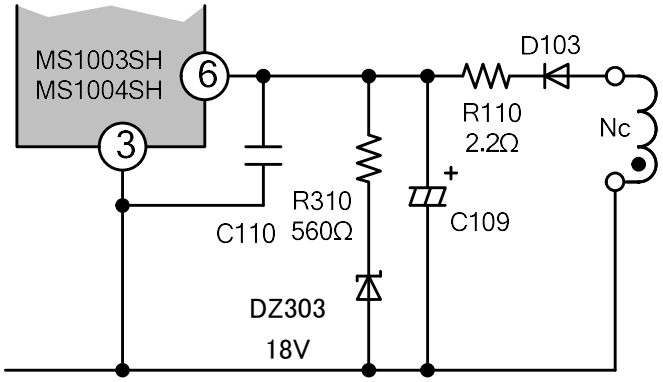
If the VCC voltage is not well regulated due to design conditions, such as the load specification, add R110 as shown below to the left. This is generally the most cost-effective way to improve regulation. The chart to the right shows model lines of VCC voltage regulation relative to output power. The narrow line represents VCC voltage regulation with the basic circuit (1). The bold line represents the VCC voltage regulation achieved by Measure ①.





(3) Measure ② for Poor VCC voltage regulation

The diagram below shows a circuit that improves regulation more effectively than measure ①.

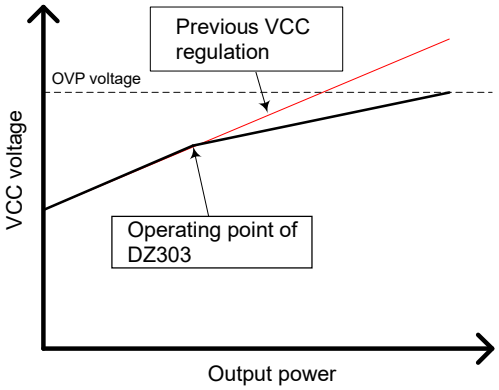


	Initial design value	Recommended value
R310	560 Ω	220 Ω–1 kΩ
DZ303	18 V	16 V–22 V

* Keep in mind potential losses associated with R310.

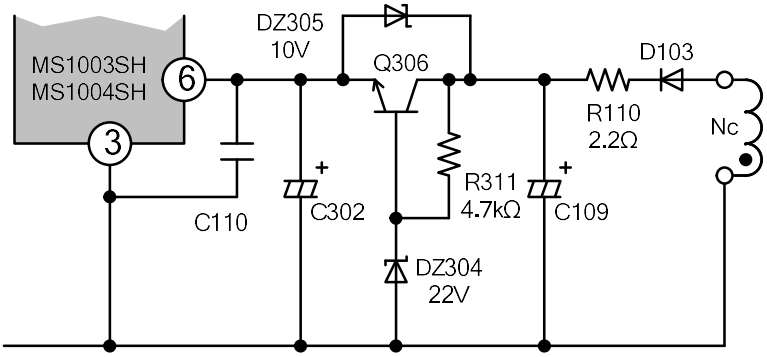
This measure will improve the regulation (represented by the narrow line) and move it to the bold line on the chart to the right. The voltage setting of DZ303 is the operating point of DZ303, as shown to the right.

This circuit incorporating this measure is the most effective circuit available when using super standby mode. No losses occur in super-standby mode.
The bold line represents the VCC voltage regulation achieved by Measure ②.



(4) Measure ③ for Poor VCC voltage regulation

If the countermeasures described in measure ② and ③ above are not effective, use the dropper circuit shown below to stabilize VCC. Use the constants given below as guidelines.

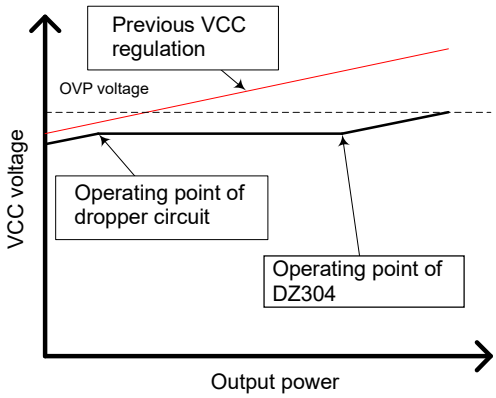


When selecting DZ304, note the withstand voltage between Q306 and EB.
If the withstand voltage between Q306 and EB is 5 V, select 22 V or greater.
If the withstand voltage between Q306 and EB is 7 V, select 20 V or greater.

This measure stabilizes VCC to the zener voltage of DZ304 plus VBE of Q306. Unless DZ304 is added as shown in the diagram above, OVP of the VCC pin cannot be used. Set the zener voltage of DZ304 so that the OVP functions properly.

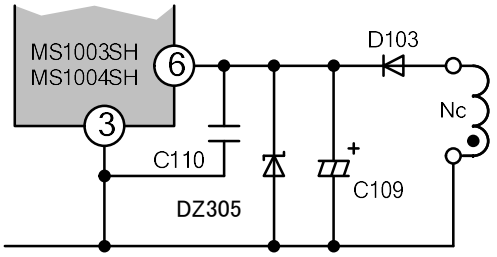
The chart to the right shows a VCC regulation model after implementing the measures above. Activating the dropper circuit stabilizes the voltage. When DZ304 activates, the voltage becomes the OVP voltage.

The bold line represents the VCC voltage regulation achieved by Measure ③.



(5) Circuit protection

The VCC pin may break down during a short circuit test. If so, protect the circuit using a zener diode (DZ305), as shown to the right. A zener diode for 30 V or greater should have negligible effect on IC functions for normal use.



5.5.6 Setting resonating capacitor

The capacitance set for the resonating capacitor should be between 100 pF and 3300 pF for real-world applications. No other restrictions apply.

(1) Conditions under which a relatively large capacitance is selected

- The quasi-resonance bottom is close to 0V because, for example, input voltage is low and the main switching device loss is expected to be very small.
- The conducted emissions are high.
- The surge voltage is large relative to the withstand voltage of the main switching device, and there is no margin.

(2) Conditions under which a relatively small capacitance is selected

- The main switching device generates significant heat.
- Standby power must be minimized.

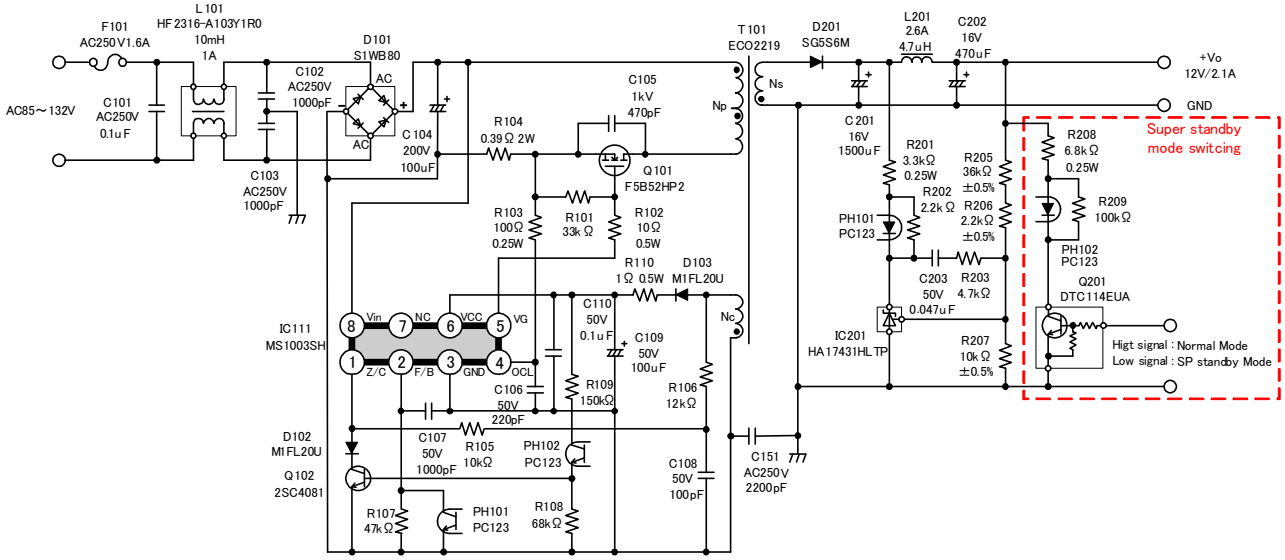
The following table lists the effects of changes in the capacitance of the resonating capacitor on power supply performance.

Item	Reduce capacitance.	⇔	Increase capacitance.
Main switching device peak voltage	Rise	⇔	Fall
Drooping-point power	Increase	⇔	Decrease
Heat buildup in the main switching device	Decrease	⇔	Increase
Main switching device current immediately after powering on	Decrease	⇔	Increase
Main switching peak current under the same output power conditions	Decrease	⇔	Increase
Regulation of Vo	Decline	⇔	Improve
Regulation of VCC	Decline	⇔	Improve
Power supply efficiency	Improve	⇔	Decline
Noise	Rising tendency	⇔	Declining tendency

In efforts to optimize power supply performance, changes in the capacitance of the resonating capacitor often involve trade-offs. Carefully examine the advantages and disadvantages of the change when determining the constants. It may be possible to improve the trade-offs by redesigning the transformer. Consider redesigning the transformer to optimize power supply performance.

6. Example circuit diagram

6.1 Circuit diagram



This circuit is based on the results of calculations described in Section 6.2 below. Actual values may differ from calculations due to differences in efficiency and in the response system, variance in IC thresholds, temperature drifts for each component, and various other factors. Use the results of calculations as guidelines. In the example circuit, the OCL resistance ($R_{(OCL)}$) is changed from 0.37 Ω to 0.39 Ω due to discrepancies between the actual device and calculations. The transformer inductance at AL-value = 140 has been changed from 0.656 mH to 0.647 mH based on information from the transformer manufacturer.

6.2 Calculations for example circuit design

This section discusses the design procedure for the example circuit shown in Section 6.1.

(1) I/O specification and transformer

Control IC	MS1003SH
Input specification	AC85–132 V
Output specification	12V/2.1 A
Transformer	ECO2219 (TDK)

(2) Initial design value list

$V_{DC(min)}$	102V	D	0.47	Cq	470 pF
$V_{DC(max)}$	187V	Po	25.2 W	P_L	1.2×Po W
f(min)	50 kHz	η	0.85	Ae	46.4 mm^2
V_{O1}	12V	V_{NC}	15 V	ΔB	300 mT
V_{o1} rectification diode forward voltage: V_{F1}					0.8 V
V_{NC} rectification diode forward voltage: V_{FNC}					0.6 V

◆Setting the on duty ratio (D)

The on duty ratio D is determined primarily by the withstand voltage of the main switching device and the corresponding heat buildup. The following table lists changes in characteristics resulting from changes in D.

On duty ratio (D)	Decrease	⇔	Increase
Voltage applied to the main switching device	Fall	⇔	Rise
Main switching device peak current	Increase	⇔	Decrease
Main switching device switching loss	Increase	⇔	Decrease
Main switching device conduction loss	Increase	⇔	Decrease
Operating frequency fluctuation range	Decrease	⇔	Increase

(3) Calculating the primary inductance : Lp and the main switch peak current : I_{DP}

Substitute

Formula 4: $t_{on(\max)1} = \dfrac{0.47}{50\times10^{3}}$ = 9.4μs and

Formula 9: $I_{DP} = \dfrac{2\times25.2\times1.2}{0.85\times102\times0.47}$ = 1.484A into Formula 10.

Formula 10: $Lp = \dfrac{102\times9.4\times10^{-6}}{1.484}$ = 0.646mH

(4) Calculating the number of turns in the primary winding : Np

Substitute

Formula 4: $t_{on(\max)1} = \dfrac{D}{f_{(\min)}} = \dfrac{0.47}{50\times10^{3}}$ = 9.4μs into Formula 11.

Formula 11: $Np = \dfrac{V_{DC(\min)}\cdot t_{on(\max)1}\cdot10^{7}}{\Delta B\cdot Ae} = \dfrac{102\times9.4\times10^{-6}\times10^{7}}{300\times0.464}$ = 68.8 turns

Round the result to the nearest integer, i.e., Np = 68 turns.

(Round up the result when adjusting D upwards. In the example, the result is rounded down to adjust it downwards.)

(5) Calculating the number of turns in the control output winding : N_{S1}

Formula 6: $tq = 3.14\cdot\sqrt{0.646\times10^{-3}\times470\times10^{-12}}$ = 1.73μs

Formula 13: $N_{S1} = \dfrac{(12+0.6)\times68\times(\dfrac{1}{50\times10^{3}} - 9.4\times10^{-6} - 1.73\times10^{-6})}{102\times9.6\times10^{-6}}$ = 7.76 turns

Round the result to the nearest integer, i.e., N_{S1} = 8 turns.

(Round down the result when adjusting D upwards. In the example, the result is rounded up to adjust it downwards.)

(6) Calculating the number of turns in the control winding : Nc

Formula 15: $Nc = 8 \times \frac{15 + 0.8}{12 + 0.6} = 10.03$ turns

Round the result to the nearest integer, i.e., Nc = 10 turns.

(Round up the result when adjusting the voltage upwards. When adjusting it downwards, round it down.)

(7) Recalculating the transformer design

The actual design values of a transformer differ from initial design values because results are rounded to integers during the design process and because actual resistances and inductances differ from calculations.

The differences are corrected and the OCL resistance $R_{(OCL)}$ and transformer core gap are determined as follows:

1) Correcting the main switching peak current and determining OCL resistance $R_{(OCL)}$

Calculate $R_{(OCL)}$ based on the relationship between the main switching peak current obtained in Section (3) and the VTH (OCL) clamp.

$$R_{(OCL)} = \frac{0.54}{1.484} = 0.3638\,\Omega$$

To adjust resistance, change $R_{(OCL)}$ to 0.37 Ω (e.g., 0.22 Ω + 0.15 Ω).

The main switching peak current changes to $I_{DP} = \frac{0.54}{0.37} = 1.46$ A.

2) Determining the core gap and correcting the inductance

To specify the core gap when ordering a transformer, you can use the result of Formula 12 in section 5.3. Note that using the inductance coefficient “AL-value” is more common.

The AL-value is among the key parameters that determine transformer core performance, together with the NI-limit expressed in $[\frac{nH}{N^2}]$ and magnetic saturation condition.

The inductance is corrected based on the assumption that the AL-value is 140.
(Standard AL-values vary from manufacturer to manufacturer. Contact the transformer manufacturer to obtain more information.)

Since $\text{AL - value} = \frac{nH}{N^2}$, the result is $140 \times 68^2 = 647360$ nH.

The inductance Lp is corrected to 0.647 mH.

3) Correcting initial design values

From the I_{DP} and Lp obtained in Sections 1) and 2), the initial design values are corrected as follows:

Formula 10: $t_{on(\max)l} = \frac{Lp \cdot I_{DP}}{V_{DC(\min)}} = \frac{0.647 \times 10^{-3} \times 1.46}{102} = 9.26$ µs

Formula 6: $tq = 3.14 \cdot \sqrt{0.647 \times 10^{-3} \times 470 \times 10^{-12}} = 1.73\ \mu s$

Formula 5: $t_{off\,(\max)} = \dfrac{8 \times 102 \times 9.26 \times 10^{-6}}{68 \times (12 + 0.6)} + 1.73 \times 10^{-6} = 10.55\ \mu s$

On duty ratio: $D = \dfrac{t_{on(\max)1}}{t_{on(\max)1} + t_{off\,(\max)}} = \dfrac{9.26}{9.26 + 10.55} = 0.467$

Minimum oscillation frequency: $f_{(\min)} = \dfrac{1}{t_{on(\max)1} + t_{off\,(\max)}} = \dfrac{1}{9.26 + 10.55} = 50.48\ kHz$

Formula 9: $P_L = \dfrac{I_{DP} \cdot \eta \cdot V_{DC(\min)} \cdot D}{2} = \dfrac{1.46 \times 0.85 \times 102 \times 0.467}{2} = 29.56\ W$

The preceding calculation shows that the droop point power is 1.173 times the maximum power; i.e., $P_L = 1.173 \cdot P_{O(\max)}$.

The following formula gives ΔB:

$$\Delta B = \frac{V_{DC(\min)} \cdot t_{on(\max)1} \cdot 10^7}{Np \cdot Ae} = \frac{102 \times 9.26 \times 10^{-6} \times 10^7}{68 \times 0.464} = 299.35\ mT$$

The result indicates whether ΔB presents any problems.

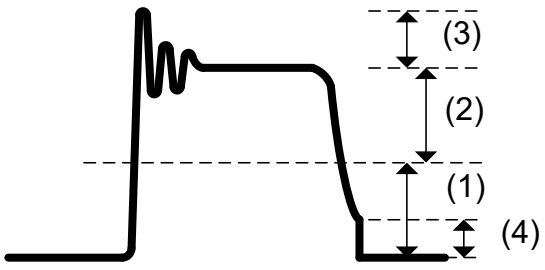
◆Corrected parameters

f(min)	50.48 kHz	D	0.467	Δ B	299.4 mT
Lp	0.647 mH	tq	1.73 μs	PL	1.173×Po W
Np	68 turns	NS1	8 turns	Nc	10 turns

Check to determine whether these corrected values are adequate. In particular, make sure P_L is not too large (the output current is not too large) or too small (there is sufficient margin relative to load) and that the resulting conditions do not lead to saturation of ΔB.

(8) Estimating the voltage applied to the main switching device

After finalizing the transformer design, estimate the withstand voltage of the main switching device and check to determine whether the selected main switching device has sufficient withstand voltage. The diagram to the right shows a model waveform of the main switching device when the main switching device is off. The maximum voltage of the main switching device is estimated by calculating (1) to (4).



1) V_{DC}

   This is the same as the input capacitor voltage. Formula 2 gives the maximum value. In this example, the maximum value is 186.7V.

2) Flyback voltage

   This is the transformer's flyback voltage: $\frac{Np \cdot (V_{O1} + V_{F1})}{N_{S1}}$

   The following formula gives the voltage: $\frac{68 \cdot (12 + 0.6)}{8}$ =107.1 V

3) Surge voltage

   This surge voltage attributable to leakage inductance varies from specification to specification and from transformer to transformer. In this example, it is estimated to be 150 V at maximum. This parameter must be confirmed using actual equipment.

4) Quasi-resonance bottom voltage

   The higher this voltage, the greater the switching loss. This is obtained by subtracting (2) from (1) above. In this example, it is 186.7 V – 107.1 V = 79.6 V.

The maximum voltage of the main switching device is 186.7 V + 107.1 V + 150 V = 443.8 V. For instance, a MOSFET capable of withstanding 500 V is suitable for use with a margin exceeding 10% (450 V). If the withstand voltage is too low, reduce on duty ratio D. Increase the on duty ratio D to make the most of quasi-resonance effects.

(8) Checking operating points

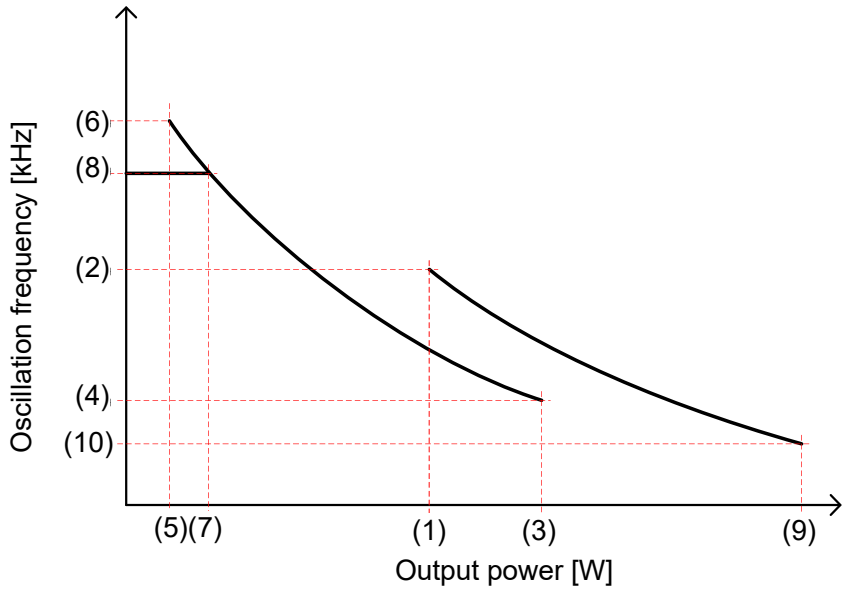
When checking the operating points, use the design values corrected in Section 6.2 (7)-3).

Work out the operating points of the example power supply in accordance with Section 5.4.

The following table gives the results of calculations based on an input voltage of DC 120 V:

(1)	Bottom-skip start power	9.33 W
(2)	Oscillation frequency at bottom-skip start	133.3 kHz
(3)	Bottom-skip end power Bottom-skip end power 1 from Formula 25 of [Condition 1] ..... 16.23 W As DC120 V = V_{DC} < $V_{DC\ (clamp)}$ = 129.4 V; Bottom-skip end power 2 from Formula 30 of [Condition 2]-1) ..... 26.77 W Bottom-skip end power 1 < Bottom skip end power 2 Bottom-skip end power 1 is used.	16.23 W
(4)	Oscillation frequency at bottom-skip end Calculated from Formulas 22 and 23 for bottom-skip end power 1.	60.74 kHz
(5)	Auto burst start power	0.62 W
(6)	Oscillation frequency immediately before auto-burst start	151.86 kHz
(7)	Auto-burst end power	1.03 W
(8)	Oscillation frequency immediately after auto-burst end	141.87 kHz
(9)	Drooping-point power Calculated from Formula 30 as DC120 V = V_{DC} < $V_{DC\ (clamp)}$ = 129.4 V.	31.8 W
(10)	Oscillation frequency at drooping-point	54.3 kHz

The chart below shows a model of the operating frequency characteristics relative to output power indicating each operating point. Check the operating points (1) to (10).



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