CAT.No.1H1201-0E

High-Side/Low-Side Driver IC

MCZ5606SC
MCZ5607SC

Application Note
Version 1.0

Usage Precautions

Thank you for purchasing this Shindengen product.

Note the following warnings and precautions to ensure safety when using this IC:

WARNING	⚠	• Indicates hazards that may lead to death, serious injury, or serious damage to property if the product is handled improperly.
CAUTION	⚠	• Indicates hazards that may lead to minor injury or minor damage to property if the product is handled improperly.

WARNING	⚠	• This IC is intended for use in general electronic devices (e.g., office equipment, communications equipment, measuring equipment, domestic appliances). Do not use in mission critical control equipment for which malfunctions or failure may result in death; examples include medical equipment, aerospace equipment, rail vehicles, transportation equipment (e.g., vehicle-mounted, marine), and nuclear power control equipment. Please consult with Shindengen regarding use in equipment other than general electronic devices.
CAUTION	⚠	• Never attempt to repair or modify the product. Doing so may lead to serious incidents or injury, ***including electric shock, damage, fire, and malfunctions***.
	⚠	• Excessively high or reduced voltages may be produced at the output pins under abnormal conditions. Protective measures (e.g., overvoltage and overcurrent safeguards) should be incorporated into the final device to protect against possible load malfunctions and damage under abnormal conditions.
	⚠	• Check the polarity of the input and output pins to ensure that they are properly connected before supplying power. ***Failure to do so may trip protective devices or lead to smoke generation or fire.***
	⚠	• Use only the specified input voltage. Be sure to incorporate protective devices on the input line. ***Failure to do so may result in smoke generation or fire under abnormal conditions.***
	⚠	• In the event of a failure or abnormality during use, shut off the input immediately and turn off the power supply, then promptly contact Shindengen.

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- Confirm the issued specifications for the product before use.
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⚠ Shindengen strives constantly to improve product quality and reliability. Nevertheless, all semiconductor products are subject to occasional failures or malfunctions. The user is responsible for safeguarding against accidents causing injury or death, fire, and social harm through the use of redundancy, fire prevention, and malfunction prevention design.

⚠ The Shindengen semiconductor products described in this document are not designed or manufactured for use in equipment or systems subject to the stringent quality and reliability requirements of mission critical systems in which failures or malfunctions may pose direct consequences for human life or health. Be sure to contact Shindengen and obtain confirmation before using the products in equipment or systems corresponding to the following specific applications:

Special uses	Transportation equipment (e.g. vehicle-mounted, marine), core communications equipment, traffic signal equipment, disaster prevention/security equipment, various safety equipment, medical equipment, etc.
Specified uses	Nuclear power control systems, aviation equipment, aerospace equipment, undersea repeater equipment, life support equipment, etc.

⚠ Even for IC products that do not correspond to the specific uses described herein, contact Shindengen if you intend to use our products in equipment or systems designed to operate continuously or equipment or systems that require long product service life.

Contents

1. Overview

The MCZ5606SC and MCZ5607SC are two-input/two-output high-side/low-side driver ICs for driving power devices such as power MOSFETs and IGBTs. They incorporate a 622 V withstand voltage level shift circuit and a 22 V withstand voltage driver. They are suitable for use in a wide range of applications, including inverter circuits and AC/DC or DC/DC power supplies.

They incorporate a simultaneous ON prevention protection function to prevent through current occurring by canceling the output if ON signals are input to two input pins simultaneously.

1.1 Features

The main MCZ5606SC/MCZ5607SC features are as follows:

- High-side withstand voltage: 622 V
- 2-input/2-output high-side/low-side driver
- Source current I_source = 220 mA, sink current I_sink = 450 mA
- ton = 240 ns, toff = 270 ns, tr = 75 ns, tf = 30 ns
- Supports both input 5 V and input 3.3 V logic
- Incorporates UVLO/simultaneous ON prevention protection function
- High-side dVS/dt tolerance: 50 V/ns
- The MCZ5606SC and MCZ5607SC have different pin assignments. (See page 4.)

1.2 Standard circuit diagram

An example of a standard half-bridge circuit diagram is shown below.

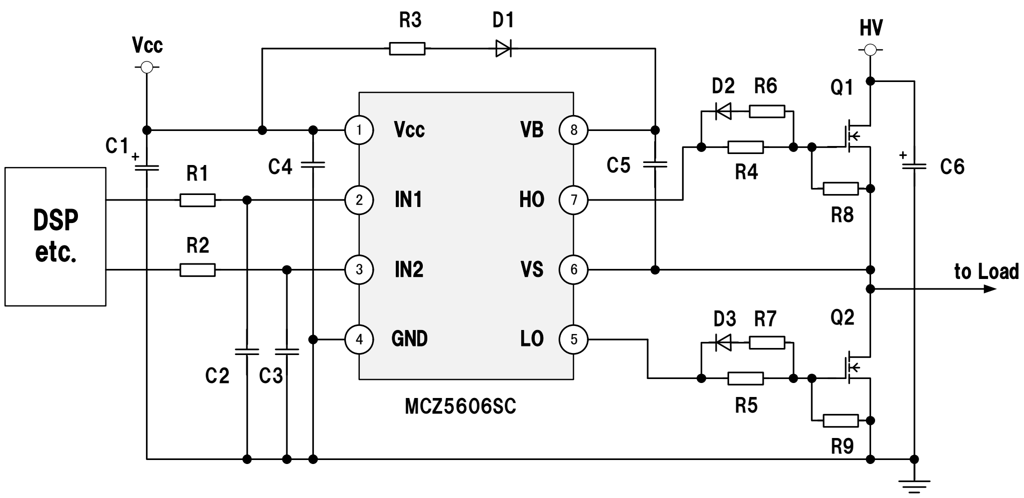
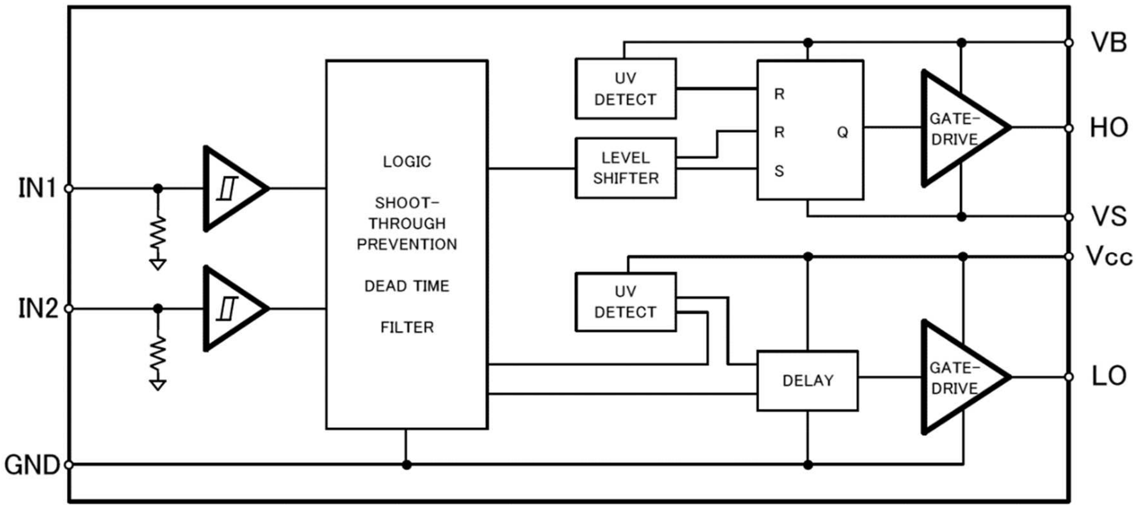


Figure 1 Standard half-bridge circuit (example using MCZ5606SC)

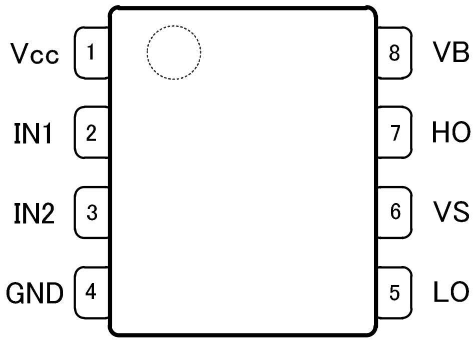
1.3 Block diagram

・MCZ5606SC / MCZ5607SC



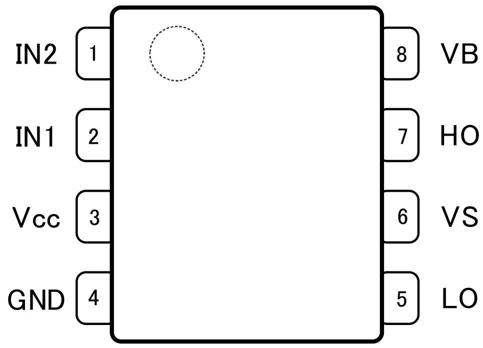
1.4 Pin assignment diagram

・MCZ5606SC



Package：SOP8J

・MCZ5607SC



Package：SOP8J

1.5 Pin function list

・MCZ5606SC

Pin No.	Symbol	Name
1	Vcc	Input terminal for power supply
2	IN1	Input1 terminal
3	IN2	Input2 terminal
4	GND	Ground terminal
5	LO	Driver2 output terminal
6	VS	Driver1 ground terminal
7	HO	Driver1 output terminal
8	VB	Driver1 input terminal for power supply

・MCZ5607SC

Pin No.	Symbol	Name
1	IN2	Input pin 2
2	IN1	Input1 terminal
3	Vcc	Input terminal for power supply
4	GND	Ground terminal
5	LO	Driver2 output terminal
6	VS	Driver1 ground terminal
7	HO	Driver1 output terminal
8	VB	Driver1 input terminal for power supply

2. Specifications

Unless otherwise specified, Tj = 25 °C, Vcc = VB = 16 V, VS = GND. IN1 = IN2 is abbreviated as IN.

The current polarity is shown as negative for current drawn in and positive for current output.

The voltages indicated are DC voltages (not AC voltages). Items in the table indicated "-" are non-guaranteed values.

2.1 Absolute maximum ratings

Exceeding the absolute maximum ratings may result in malfunction or device destruction.

Item	Symbol	Rating	Units
Thermal ratings			
Storage temperature	Tstg	-55–150	°C
Junction temperature	Tj	-40–150	°C
Total power dissipation	Pd	1.25 (*1)	W
Thermal resistance	Rth(j-a)	100 (*1)	°C/W
Input/output ratings			
Vcc maximum applied voltage	Vcc	-0.3–22	V
IN maximum applied voltage	VIN	-0.3–6.0	V
VB maximum applied voltage	VB	-0.3–622	V
VS maximum applied voltage	VS	VB-22–VB+0.3	V
VB-VS maximum applied voltage	VBS	-0.3–22	V
HO maximum output voltage	VHO	VS-0.3–VB+0.3	V
LO maximum output voltage	VLO	-0.3–Vcc+0.3	V
dVS/dt offset voltage maximum	dVS/dt	50	V/ns

*1: Glass-Epoxy Board: 114.3 mm × 76.2 mm, thickness 1.6 mm, internal copper foil size: 74.2 mm × 74.2 mm, thickness 35 um

2.2 Recommended operating conditions

Item	Symbol	Recommended value			Units
		Min	Typ	Max	
Operating temperature	Tj(ope)	-40	–	125	°C
Vcc applied voltage	Vcc	10	–	20	V
IN applied voltage	VIN	0	–	5.5	V
VB applied voltage	VB	VS+10	–	VS+20	V
VS applied voltage	VS	0	–	500	V
VB-VS applied voltage	VBS	10	–	20	V
HO output voltage	VHO	VS	–	VB	V
LO output voltage	VLO	0	–	Vcc	V

Notes: The product life depends on the condition of use even within the above operating conditions.
Using at Tj = 105 °C or less is recommended for the equipment where a long life is expected.

2.3 Electrical characteristics

Item	Symbol	Condition	Recommended value			Units
			Min	Typ	Max	
Vcc pin						
Vcc start-up voltage	Vcc_start		8.40	8.90	9.40	V
Vcc stop voltage	Vcc_stop		7.70	8.20	8.70	V
Vcc UVLO hysteresis voltage	Vcc_UVLO_Δ	Δ = Vcc_start - Vcc_stop	0.40	0.70	1.00	V
Vcc operating current	Icc	IN = 0V	170	340	680	uA
Low side minimum operating voltage (*2)	Vcc_min				5.0	V
VB pin						
VB-VS start-up voltage	VBS_start		8.40	8.90	9.40	V
VB-VS stop voltage	VBS_stop		7.70	8.20	8.70	V
VBS UVLO hysteresis voltage	VBS_UVLO_Δ	Δ = VBS_start - VBS_stop	0.40	0.70	1.00	V
VBS operating current	IBS	IN = 0V	110	220	440	uA
High side minimum operating voltage (*2)	VBS_min				5.0	V
IN1, IN2 pins						
Input upper threshold voltage	VIH		1.6	2.0	2.4	V
Input lower threshold voltage	VIL		0.8	1.1	1.4	V
Input threshold hysteresis voltage	VINhys	VINhys = VIH - VIL	0.5	0.9	1.3	V
HO, LO pins						
Output source current	IHO_H ILO_H	IN1 = 5V, HO – VS = 0V IN2 = 5V, LO - GND = 0V	160	220	280	mA
Output sink current	IHO_L ILO_L	IN1 = 0V, HO = VS = 16V IN2 = 0V, LO = GND = 16V	340	450	560	mA
Dead time	DT		90	180	270	ns
Turn-on propagation delay time	ton	CL=1000pF	120	240	360	ns
Turn-off propagation delay time	toff	CL=1000pF	130	270	410	ns
propagation delay time	DM	Δton(HS - LS) Δtoff(HS - LS)	-50	0	50	ns
Output rise time (*2)(*3)	tr	CL=1000pF		75		ns
Output fall time (*2)(*3)	tf	CL=1000pF		30		ns
Input filter time 1	tFILIN1	Positive pulse IN1,IN2			250	ns
Input filter time 2	tFILIN2	Negatve pulse IN1,IN2			350	ns
Output pulse width match	ΔPwIO	｜Pw(IN) - Pw(OUT)｜, Pw(IN) > 1us		30	120	ns

*2: Design assurance
*3: Vcc = 16 V (10 % → 1.6 V, 90 % → 14.4 V)

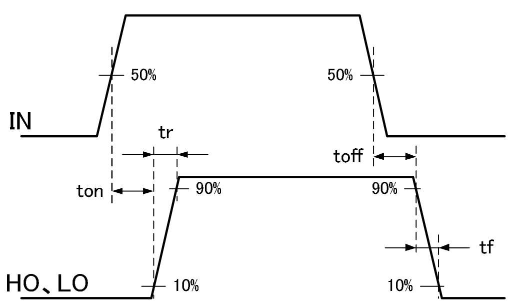


Figure 2 Definition of propagation delay time and rise/fall time

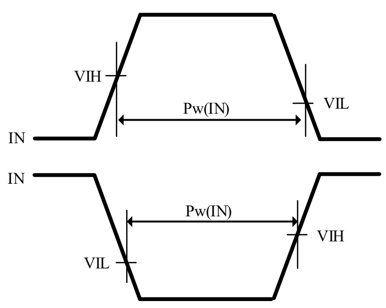


Figure 3 Definition of input pulse width Pw(IN)

2.4 Typical characteristic curves (Reference curves)

The data provided here indicate typical characteristics and do not guarantee specific characteristics.

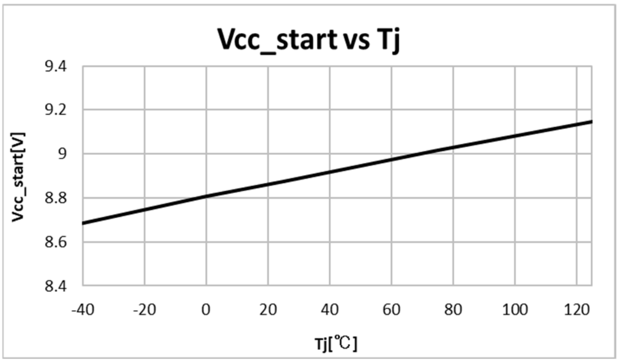


Figure 4 Vcc start-up voltage against junction temperature

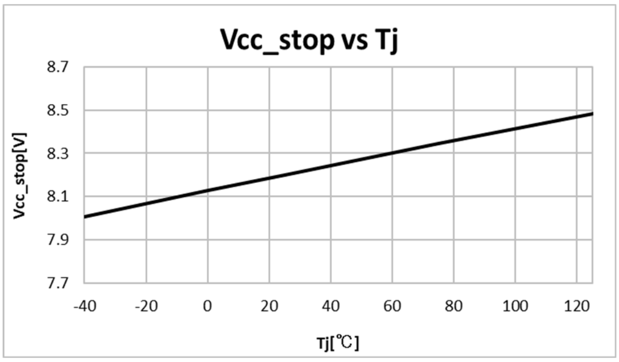


Figure 5 Vcc stop voltage against junction temperature

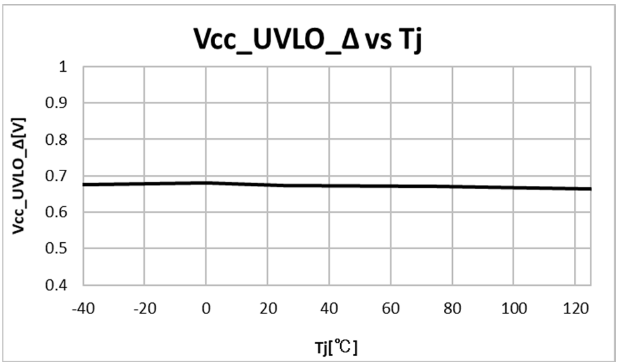


Figure 6 Vcc UVLO hysteresis voltage against junction temperature

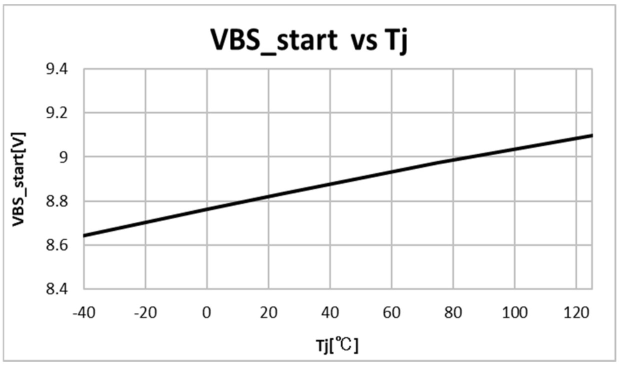


Figure 7 VB-VS start-up voltage against junction temperature

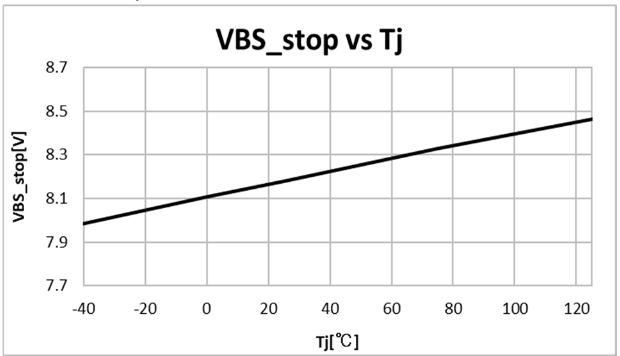


Figure 8 VB-VS stop voltage against junction temperature

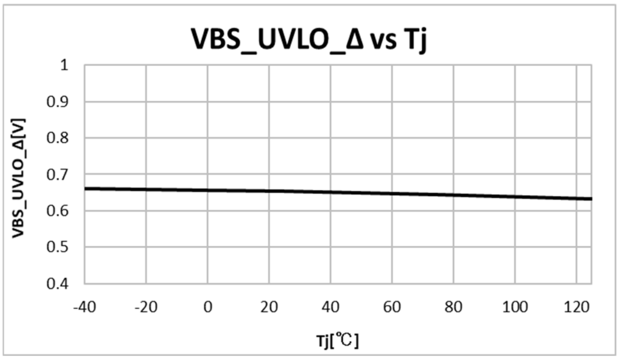


Figure 9 VBS UVLO hysteresis voltage against junction temperature

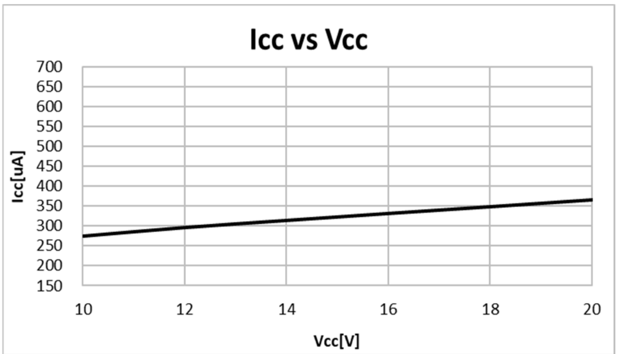


Figure 10 Vcc operating current against Vcc pin applied voltage

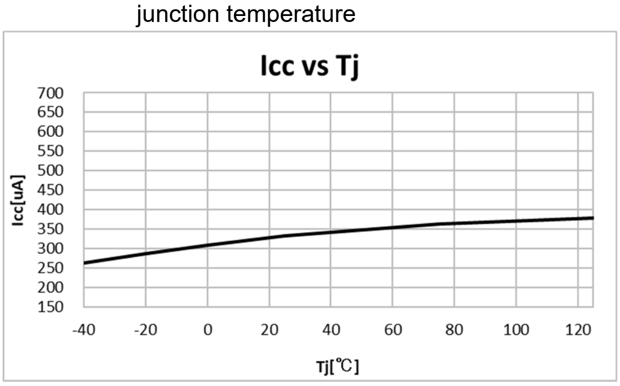


Figure 11 Vcc operating current against junction temperature

2.4 Typical characteristic curves (Reference curves)
(continued)

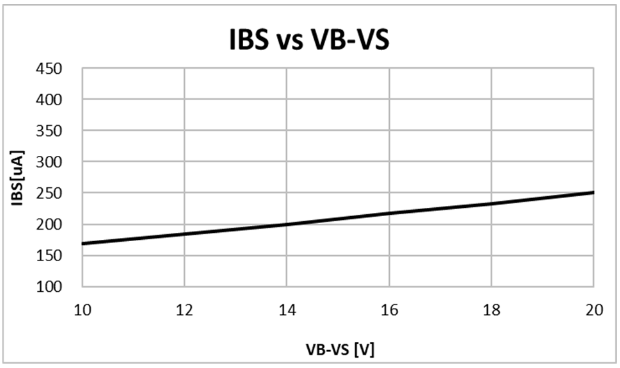


Figure 12 VBS operating current against VB-VS voltage

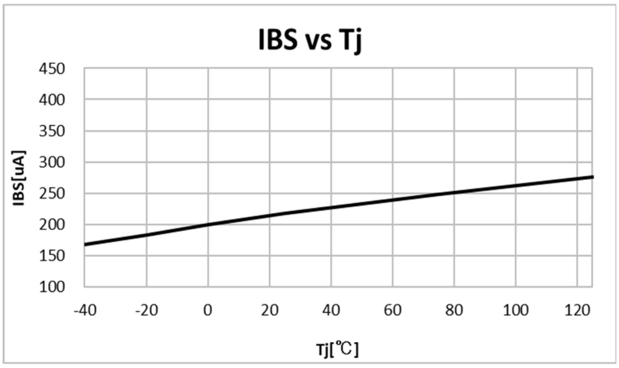


Figure 13 VBS operating current against junction temperature

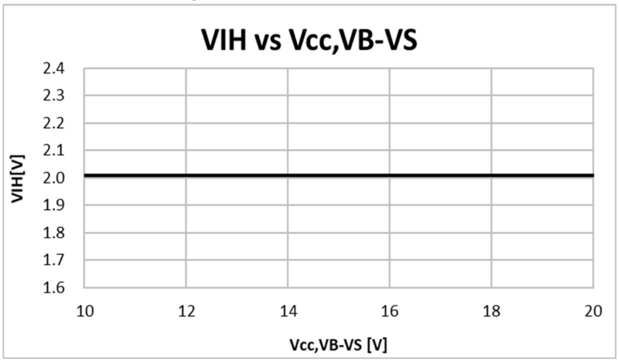


Figure 14 Input upper threshold voltage against power supply voltage

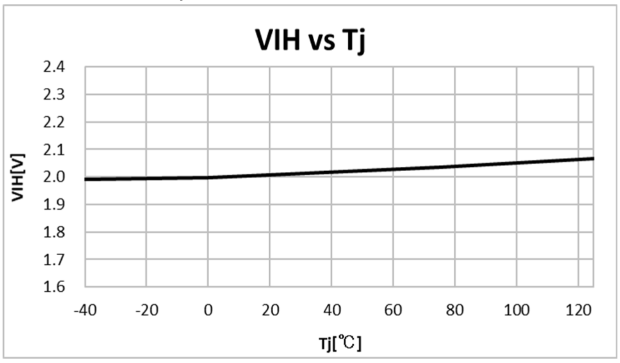


Figure 15 Input upper threshold voltage against junction temperature

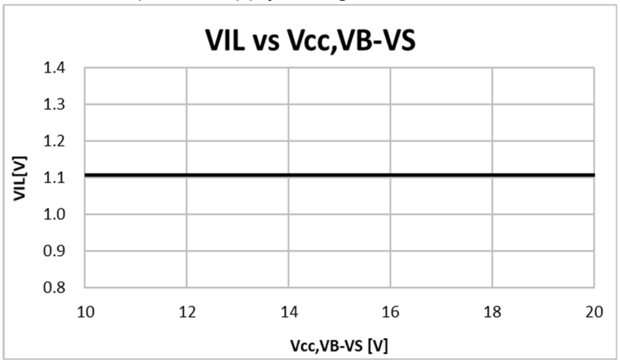


Figure 16 Input lower threshold voltage against power supply voltage

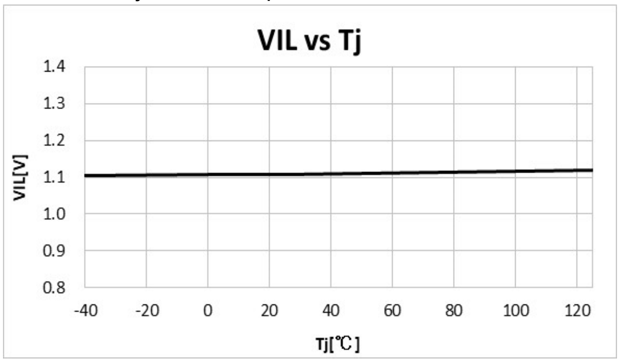


Figure 17 Input lower threshold voltage against junction temperature

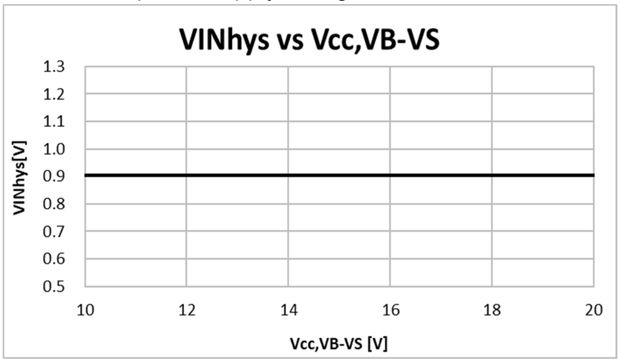


Figure 18 Input threshold hysteresis voltage against power supply voltage

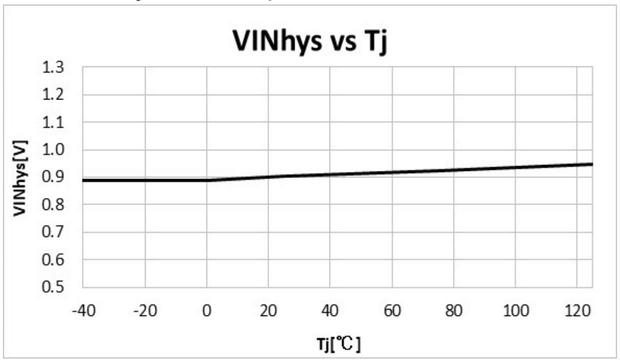


Figure 19 Input threshold hysteresis voltage against junction temperature

2.4 Typical characteristic curves (Reference curves)
(continued)

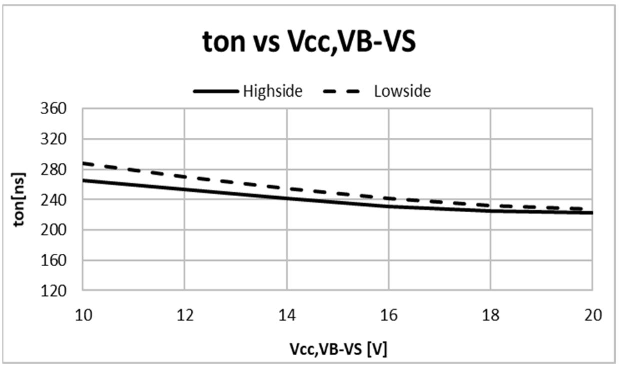


Figure 20 Turn-on propagation delay time against power supply voltage

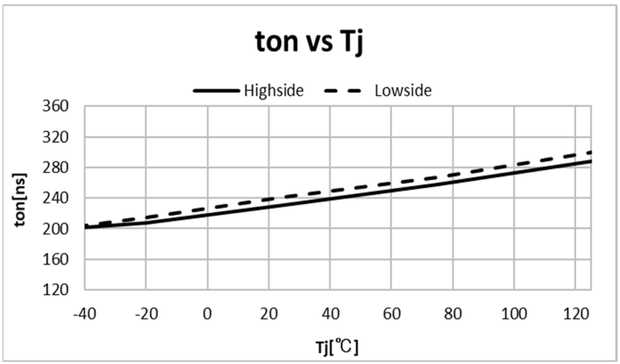


Figure 21 Turn-on propagation delay time against junction temperature

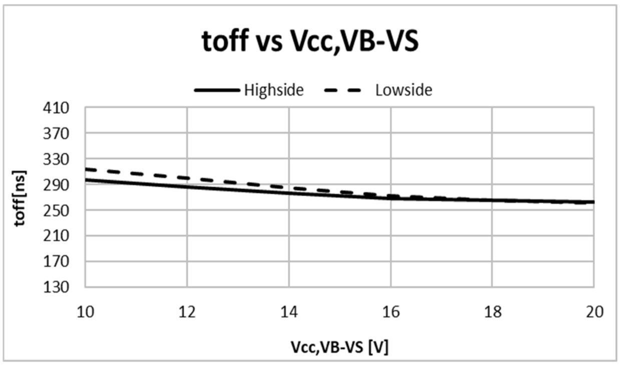


Figure 22 Turn-off propagation delay time against power supply voltage

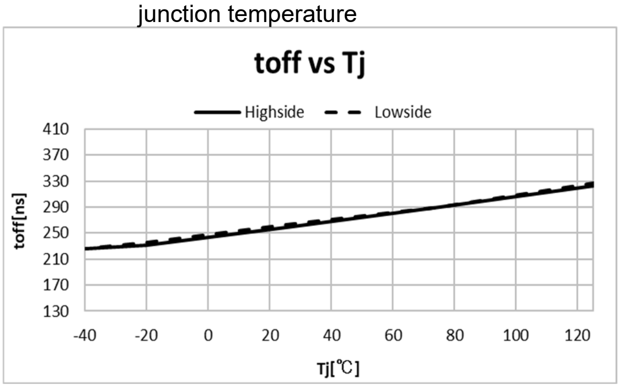


Figure 23 Turn-off propagation delay time against junction temperature

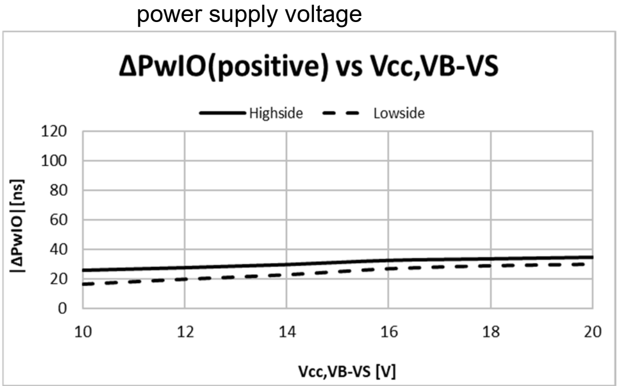


Figure 24 ΔPwIO (positive) against power supply voltage

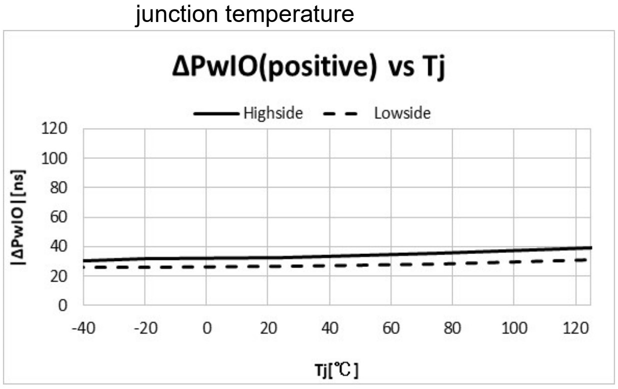


Figure 25 ΔPwIO (positive) against junction temperature

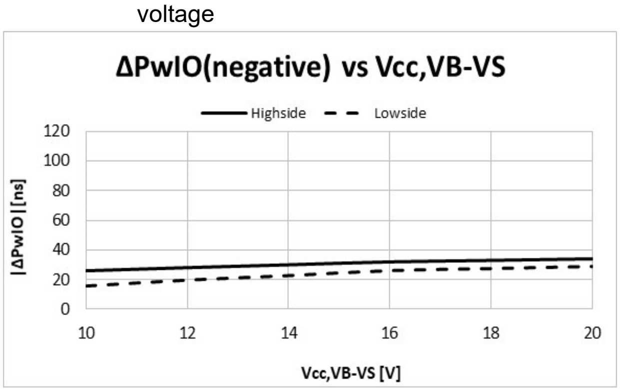


Figure 26 ΔPwIO (negative) against power supply voltage

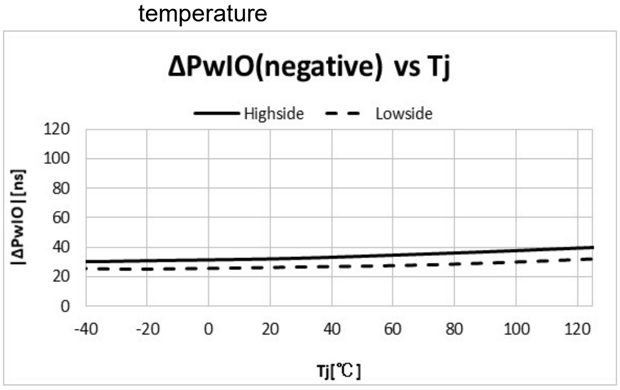


Figure 27 ΔPwIO (negative) against junction temperature

2.4 Typical characteristic curves (Reference curves)
(continued)

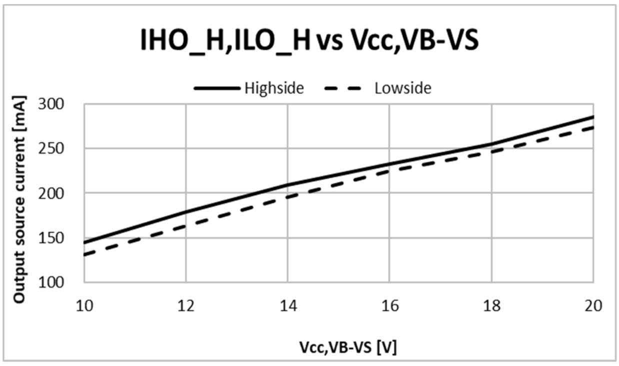


Figure 28 Output source current against power supply voltage

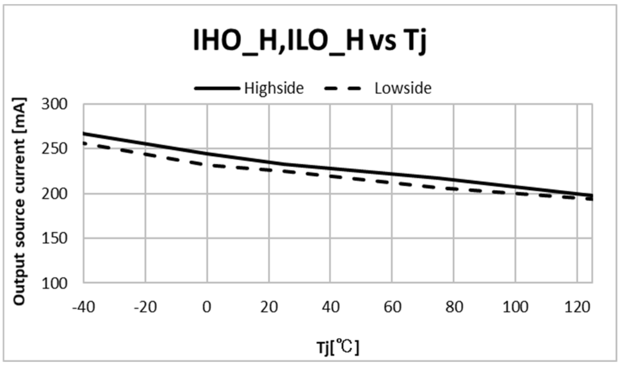


Figure 29 Output source current against junction temperature

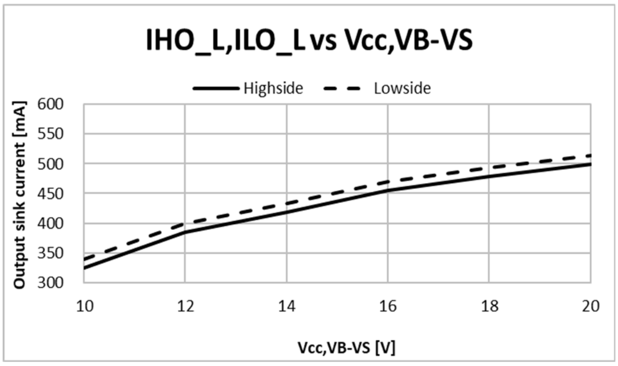


Figure 30 Output sink current against power supply voltage

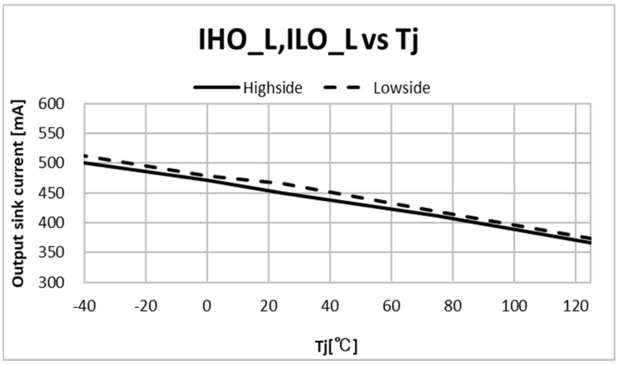


Figure 31 Output sink current against junction temperature

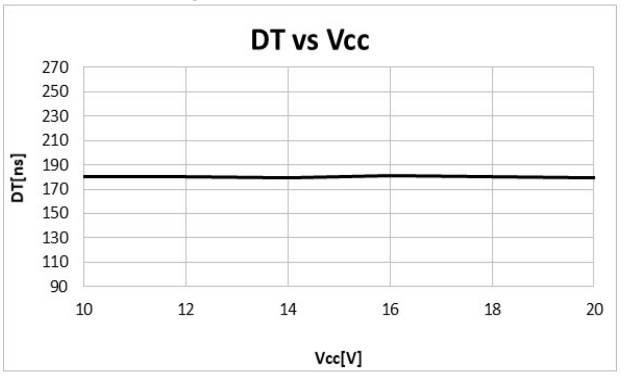


Figure 32 Dead time against Vcc applied voltage

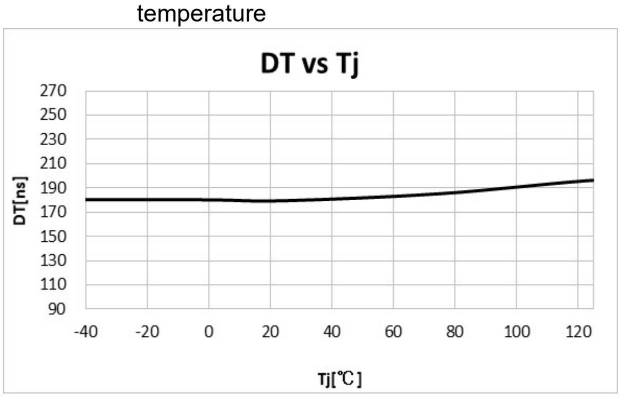


Figure 33 Dead time against junction temperature

2.5 Truth table

IN1	IN2	Vcc	VBS	HO	LO
–	–	L	L	L	L
–	–	L	H	L	L
–	L	H	L	L	L
L	L	H	H	L	L
L	H	H	L	L	H
L	H	H	H	L	H
H	L	H	H	H	L
H	H	H	L	L	L
H	H	H	H	L	L

Vcc (VBS) = H: Vcc (VBS) is Vcc_start (VBS_start) or greater or
Vcc_stop (VBS_stop) or greater after UVLO is released

Vcc (VBS) = L: Vcc (VBS) is Vcc_stop (VBS_stop) or lower or
Vcc_start (VBS_start) or lower before UVLO is released

Where

VBS: VB-VS applied voltage

After UVLO is released: A voltage of Vcc_start (VBS_start) or greater is applied

Before UVLO is released: A voltage of Vcc_stop (VBS_stop) or lower is applied at startup or after UVLO is released

3. Explanation of Functions

3.1 UVLO (Under Voltage Lock Out) function

The MCZ5606SC and MCZ5607SC incorporate a UVLO function in the power supply circuits between the Vcc and GND pins and between the VB and VS pins. (Vcc_UVLO, VBS_UVLO)

If the Vcc pin voltage is lower than the Vcc starting voltage Vcc_start at startup or lower than the Vcc stop voltage Vcc_stop after startup, the Vcc_UVLO function holds both the HO and LO output at Low, regardless of the IN1 and IN2 input signals.

The Vcc_UVLO function has a minimum operating voltage Vcc_min. The LO output is variable if the Vcc voltage is Vcc_min or lower.

If VB-VS power supply voltage VBS is lower than the VB-VS starting voltage VBS_start at startup or lower than the VB-VS stop voltage VBS_stop after startup, the VBS_UVLO function holds the HO output at Low regardless of the IN1 input signal. Note that the LO output is not held at Low by the VBS_UVLO function.

The VBS_UVLO function also has a minimum operation voltage VBS_min. If a signal is input to IN1 while the Vcc voltage is established and the VBS voltage does not exceed VBS_min, the HO output will vary.

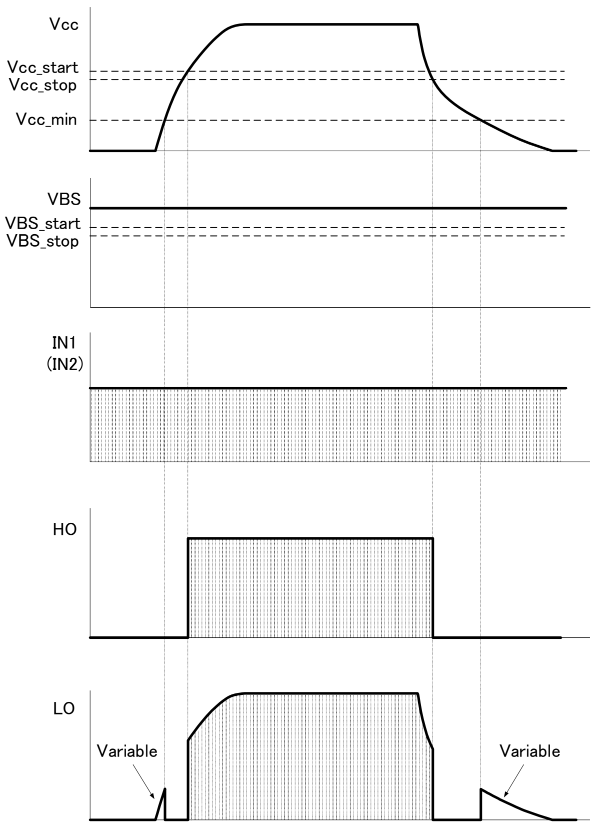


Figure 34 Vcc starting/stop sequence

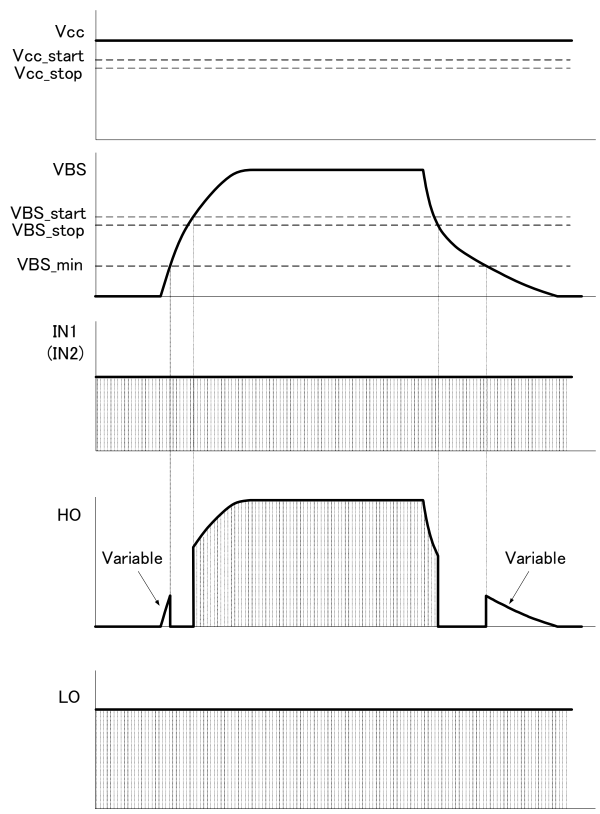


Figure 35 VBS starting/stop sequence

3.2 Simultaneous ON prevention function

The MCZ5606SC and MCZ5607SC include a simultaneous ON prevention protection function. This forces both HO and LO outputs to Low if High is simultaneously input to both the IN1 and IN2 signals.

If one of the input signals changes to Low after the simultaneous ON prevention protection function activates, the simultaneous ON prevention protection function is canceled, and the other output signal is output at High after the elapse of fixed dead time DT.

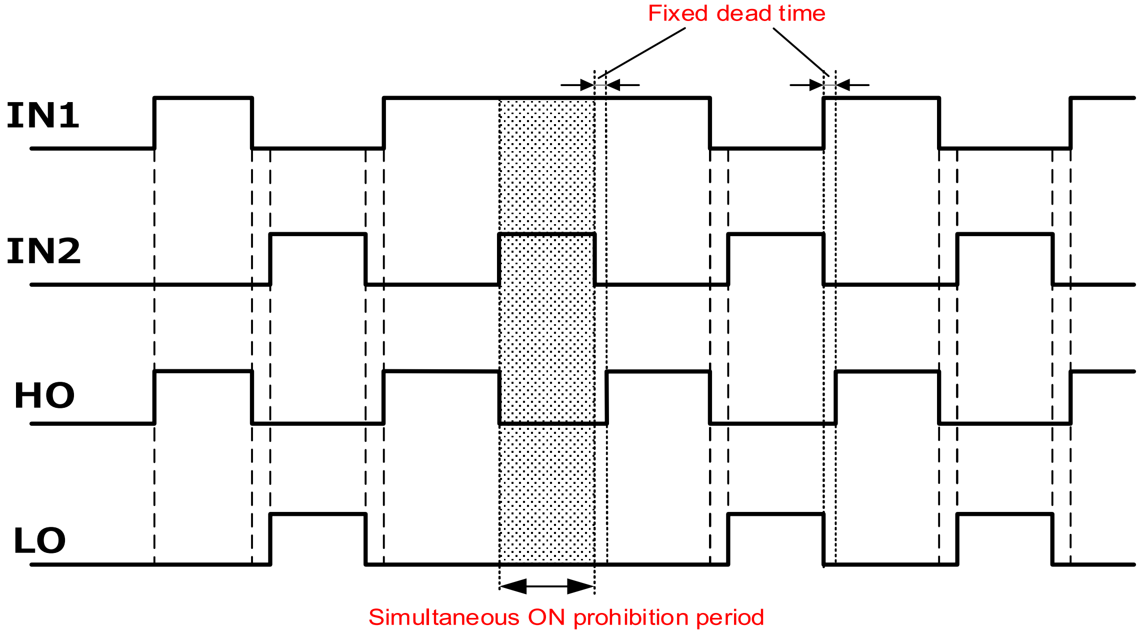


Figure 36 Simultaneous ON prevention timing chart

4. Design Precautions

The selection criteria described in this document are provided purely for guidance. Determine the appropriate parameters based on thorough evaluations on the actual apparatus.

4.1 High-side drive using a bootstrap circuit

Driving a high-side MOSFET requires a high-side power supply voltage VBS using the high-side MOSFET source potential as a reference. VBS is readily configured by mounting an external bootstrap circuit.

4.1.1 Bootstrap circuit basic operation

① When the low-side MOSFET Q2 activates, the VS voltage drops to ground potential. (The green line is at equal potential.)

② Bootstrap capacitor C5 is charged by low-side power supply voltage Vcc via bootstrap diode D1.

③ When Q2 turns off, the VS becomes a floating voltage, and the charging loop is shut off.

④ In this state, if an IN1 signal is input, the high-side MOSFET Q1 is driven by the charge stored in C5.

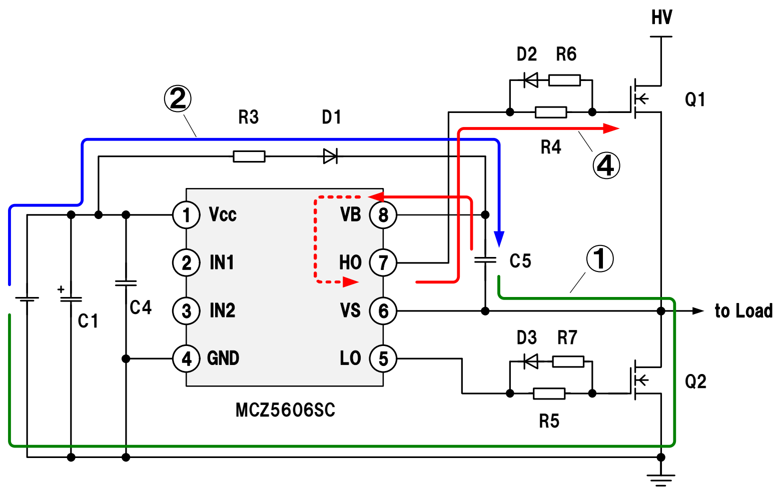


Figure 37 Bootstrap circuit basic operation (example using MCZ5606SC)

4.1.2 Bootstrap capacitor C5

C5 is not charged during the state described in 4.1.1 ④, so the high-side power supply voltage VBS gradually drops due to the Q1 gate charge current, MCZ5606SC/MCZ5607SC VBS consumption current IBS, and C5 leakage current. Select the C5 capacitance to keep VBS from dropping below the VB-VS stop voltage VBS_off while Q1 is on.

The minimum required capacitance can be obtained using equation ①, although allowing a two- to three-fold margin is recommended.

A capacitor other than an electrolytic capacitor is recommended, as this allows leakage current Icbs_leak for C5 to be ignored.

$$C5 = \frac{Qg + IBS \times Ton1(max) + Icbs\_leak \times Ton1(max)}{Vcc - VBS\_off - Vf - VLS} \quad \text{... Equation ①}$$

Where Qg: MOSFET or IGBT gate charging load [C]

IBS: MCZ5606SC/MCZ5607SC VBS operating current = 220 uA(typ.)

Ton1 (max): Q1 maximum on time [s]

Icbs_leak: Capacitor C5 leakage current [A]

Vcc: Low-side power supply voltage [V]

VBS_off: VB-VS stop voltage [V]

Vf: Bootstrap diode D1 forward voltage [V]

VLS: VDS voltage when Q2 is on [V]

4.1.3 Bootstrap diode D1

To reduce the charge returned to the Vcc power supply while Q1 is on, select an FRD or SBD with a short reverse recovery time trr for bootstrap diode D1.

Select D1 with a withstand voltage not less than the withstand voltage for Q2. The average current ID1_ave [A] for D1 can be roughly determined by the product of the total Q1 gate charge Qg1 [C] and switching frequency f [Hz] (Equation ②).

Select a diode D1 with a current rating that satisfies ID1_ave.

$$ID1\_ave = Qg1 \times f \quad \text{... Equation ②}$$

4.1.4 Inrush current protection resistance R3

The inrush current protection resistance R3 must be included to protect D1 from damage due to inrush currents during initial charging of C5. To avoid exceeding the peak permissible current ID1(peak) for D1 selected in 4.1.3, select a resistance for R3 that satisfies Equation ③.

$$R3 > \frac{Vcc\_max}{ID1(peak)} \quad \text{... Equation ③}$$

Note that if R3 is too large, the charging current to C5 may be insufficient, resulting in reduced VBS. To prevent reduced VBS, the charge discharged during the Q1 on time Ton1 must be replenished during the Q2 on time Ton2. When adjusting R3, use the actual apparatus to confirm that VBS does not drop below VBS_off even for the minimum Ton2 time.

4.1.5 Precautions when driving an IGBT

If an IGBT is used for the switching device, the collector-emitter saturation voltage Vce(sat) will be highly dependent on the gate voltage. If the gate voltage is low, the saturation voltage will increase, increasing conduction losses. The recommended IGBT gate voltage is typically a minimum of 15 V. Confirm the recommended gate voltage of the IGBT used and ensure that the recommended Vcc pin voltage operating conditions are satisfied when designing the Vcc voltage and bootstrap circuit components.

4.2 Vcc capacitor

The Vcc voltage forms the low-side power supply voltage and bootstrap capacitor feed power supply. Malfunctions may occur if the Vcc voltage ripple voltage is excessive.

To stabilize the Vcc voltage, select a capacitor for the Vcc capacitor C1 with a capacitance of at least ten times that of the bootstrap capacitor C5.

4.3 Input signal dead time

For half-bridge circuits and inverter circuits, a dead time longer than the turn-off time toff must be set using the input signal in the on/off switching timing to prevent Q1/Q2 short-circuits. If the dead time is too short, Q1/Q2 short-circuits may occur, resulting in overheating and device failure.

Increasing the gate resistance will also increase the turn-off time, necessitating a longer dead time. Factors such as other drive parameters and temperature characteristics must also be taken into consideration. Set the input signal dead time based on adequate inspections using the actual apparatus.

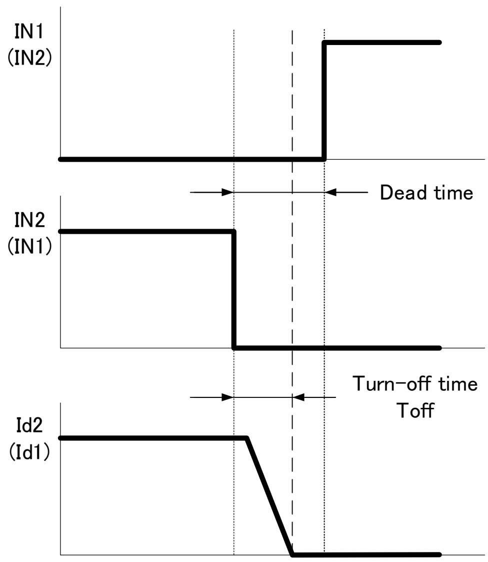


Figure 38 Relationship between dead time and turn-off time

4.4 Gate resistance

The gate resistance is affected by the MOSFET turn-on and turn-off switching characteristics. Typically, higher gate resistance for gate on Rg_source and higher gate resistance Rg_sink for gate off will increase the turn-on time and turn-off time, increasing switching losses. Similarly, a lower Rg_sink value will increase the surge voltage during switching.

Exercise care when adjusting the gate resistance to avoid both Q1/Q2 short-circuits and self turn-ons. For more information, refer to “4.3 Input signal dead time” and “4.5 Self turn-on,” respectively.

Rg_sink must be reduced to prevent Q1/Q2 short-circuits. Increase Rg_source and reduce Rg_sink when using the gate resistance to prevent self turn-on.

Additionally, adjust Rg1 and Rg2 on the actual apparatus, accounting for factors such as noise and MOSFET heat generation.

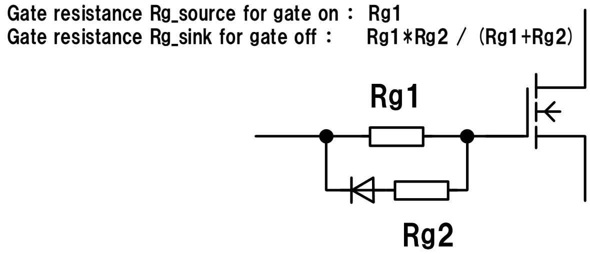


Figure 39 Gate circuit configuration example

4.5 Self turn-on

The MOSFET gate may be turned on incorrectly (self turn-on) by the dV/dt that arises when the body diode reverse recovers. The process whereby Q2 experiences self turn-on is described below.

If Q1 turns on from a state in which both Q1 and Q2 are off, the Q2 body diode BD2 reverse recovers. At the same time, dV/dt corresponding to the Q1 switching time is generated at the VS pin.

As the MOSFET includes feedback capacitance Crss, a current corresponding to Irss = Crss × dV/dt flows via the Crss of Q2.

This current Irss raises the gate potential due to the gate resistance Rg_sink, resulting in voltage Vgs between the gate and source exceeding the Q2 gate threshold voltage Vth, causing Q2 to turn on incorrectly.

This short circuits Q1 and Q2.

Measures to prevent this self turn-on include the following:

① Select a MOSFET with a small Crss/Ciss ratio.
② Add a capacitor Cgs between the gate and source.
③ Reduce the gate resistance Rg_sink.
④ Increase the gate resistance Rg_source.
⑤ Add a CR snubber between the drain and source.

These measures affect switching speed and switching losses. Always check these measures on the actual apparatus.

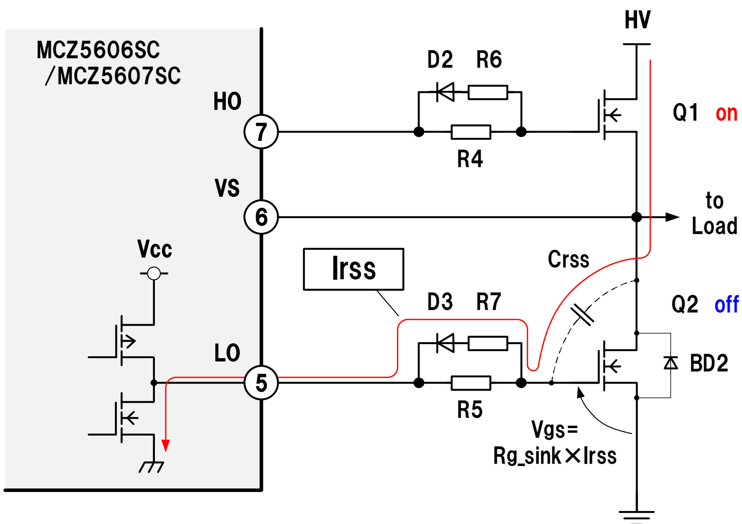


Figure 40 Self turn-on operation (Irss current path)

4.6 VS pin negative voltage

If Q1 turns off when the low-side MOSFET Q2 is off and the high-side MOSFET Q1 is on, the current flowing through Q1 refluxes between the Q2 body diode and load. In such cases, the VS pin voltage will drop with respect to GND potential due to the track inductance and current change rate di/dt. Exceeding the VS pin maximum applied voltage may result in IC malfunctions or failure.

The following are effective ways to reduce the VS negative voltage:

① Minimize track inductance by increasing the width and reducing the length of the tracks through which the reflux current flows.

In particular, increase the width and reduce the length of the Q1 source and Q2 drain tracks.

② Reduce the gate resistance Rg_sink and reduce di/dt.

Figure 41 shows an example of measurements of negative voltage tolerance with respect to negative voltage pulse width. Negative voltage tolerance here indicates the input signal value for which the IC does not malfunction or fail.

Note that Figure 41 shows typical characteristics. It makes no guarantees regarding specific values.

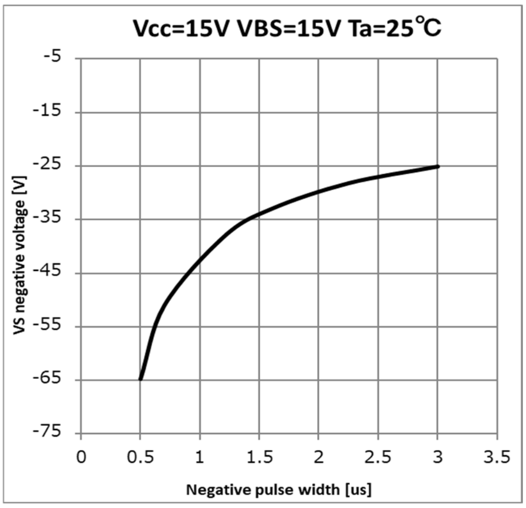


Figure 41 VS pin negative voltage tolerance (typical data)

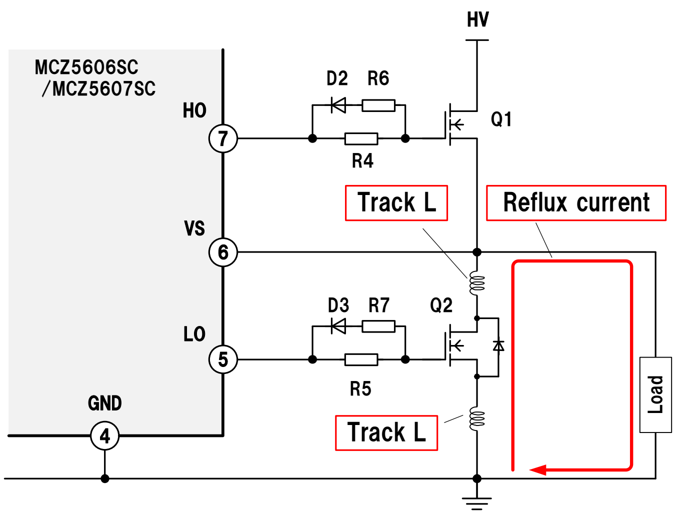


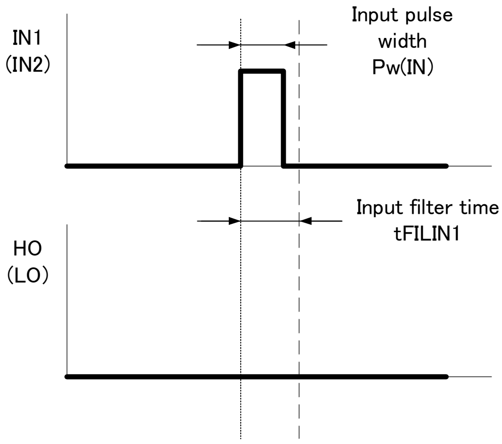
Figure 42 Track inductance and reflux current schematic

4.7 Minimum input signal pulse time

An input filter time is provided to forcibly halt the output to prevent unstable HO and LO output in cases in which input signals with an extremely short pulse are input to IN1 and IN2. The pulses applied must be at least as long as the input filter time for both the positive and negative pulses because HO and LO output will be halted if the input pulse width is shorter than the input filter time.

・ Positive pulse input

① Input pulse width < Input filter time



② Input pulse width > Input filter time

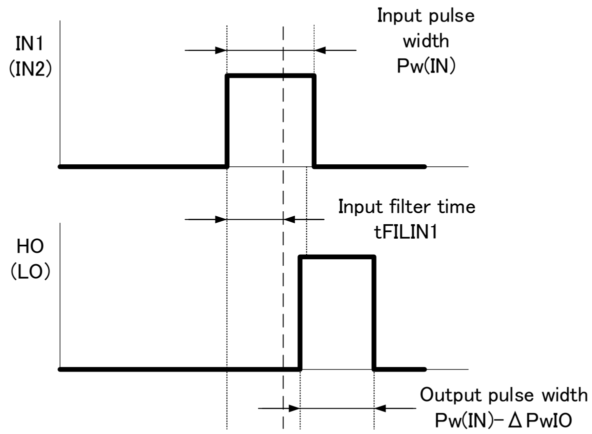
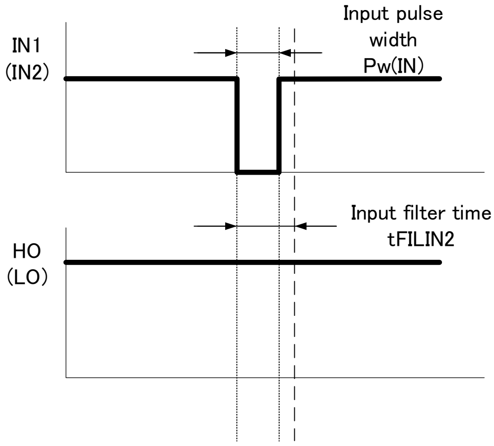


Figure 43 Minimum input signal pulse time (positive pulse input)

・ Negative pulse input

① Input pulse width < Input filter time



② Input pulse width > Input filter time

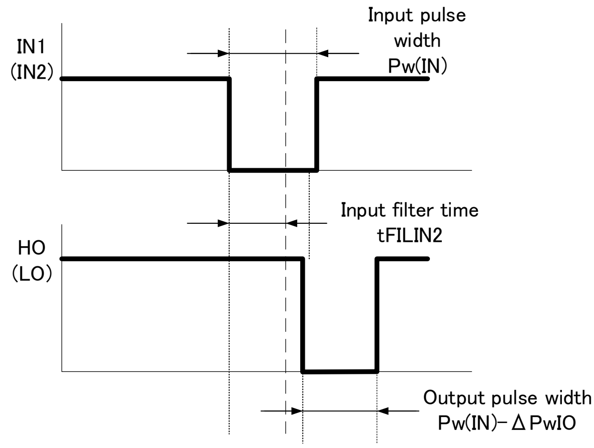


Figure 44 Minimum input signal pulse time (negative pulse input)

5. Pattern Design Precautions

This section describes the precautions required for pattern design. The actual layout must comply with the safety standards stipulated for the countries and regions in which the product is to be sold and must be thoroughly evaluated on the actual apparatus.

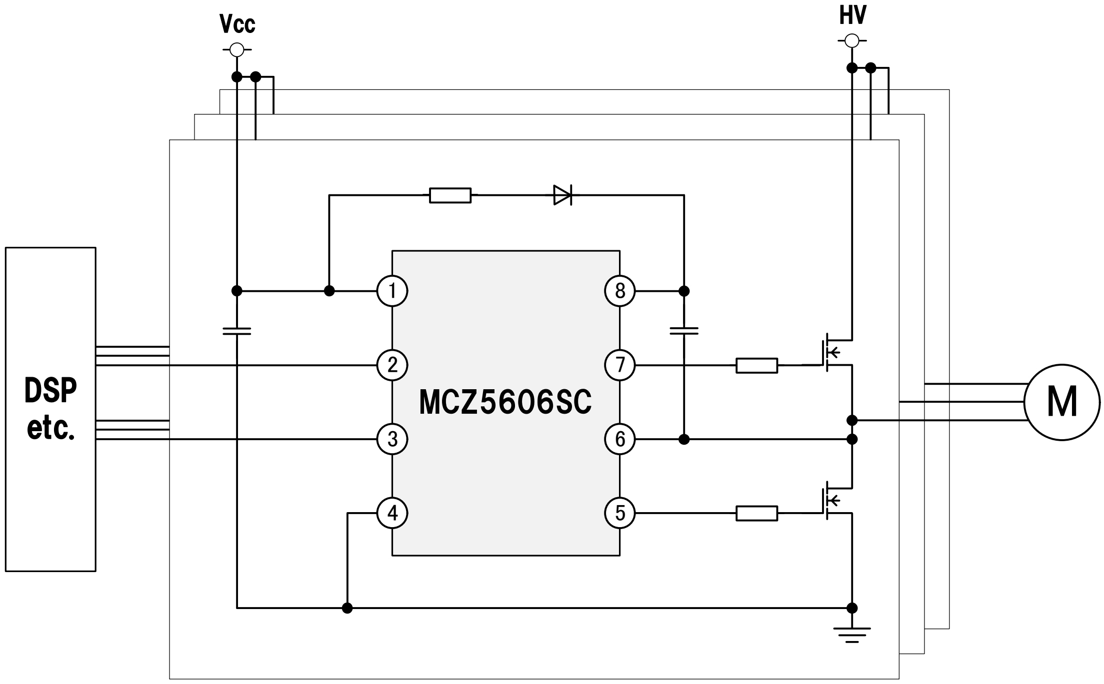
Typical pattern design should account for the following five points:

1. Design power lines carrying large current as tracks as wide and as short as possible. Separate the ground line into a power ground and IC ground. Connect the IC ground to a stable potential with minimal current fluctuations.
2. Locate the IC as close as possible to the MOSFET. Keep the drive tracks between the MOSFET gates and HO and LO as short as possible.
3. To avoid interference, design the layout to keep the drive tracks and MOSFET main circuit tracks as far apart as possible.
4. Locate Vcc capacitors C1 and C4 and the bootstrap capacitor C5 as close as possible to the MCZ5606SC/MCZ5607SC pins.
5. If the input signal is affected by external noise, we recommend locating a CR filter with a resistance between 0 Ω and several dozen Ω and capacitance of approximately 220 pF immediately next to the IN1 and IN2 pins.

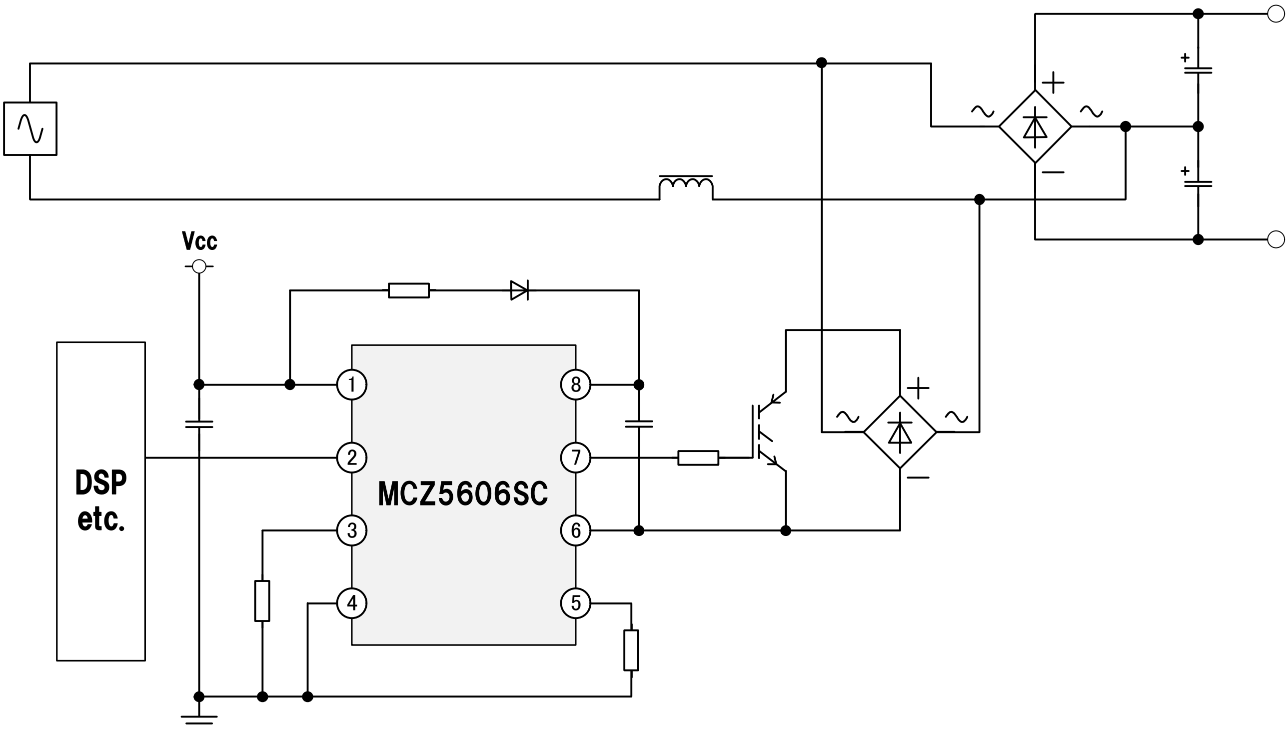
6. Example Application Circuits

This section provides examples of application circuits for which the MCZ5606SC and MCZ5607SC are suited. The examples here all use the MCZ5606SC.

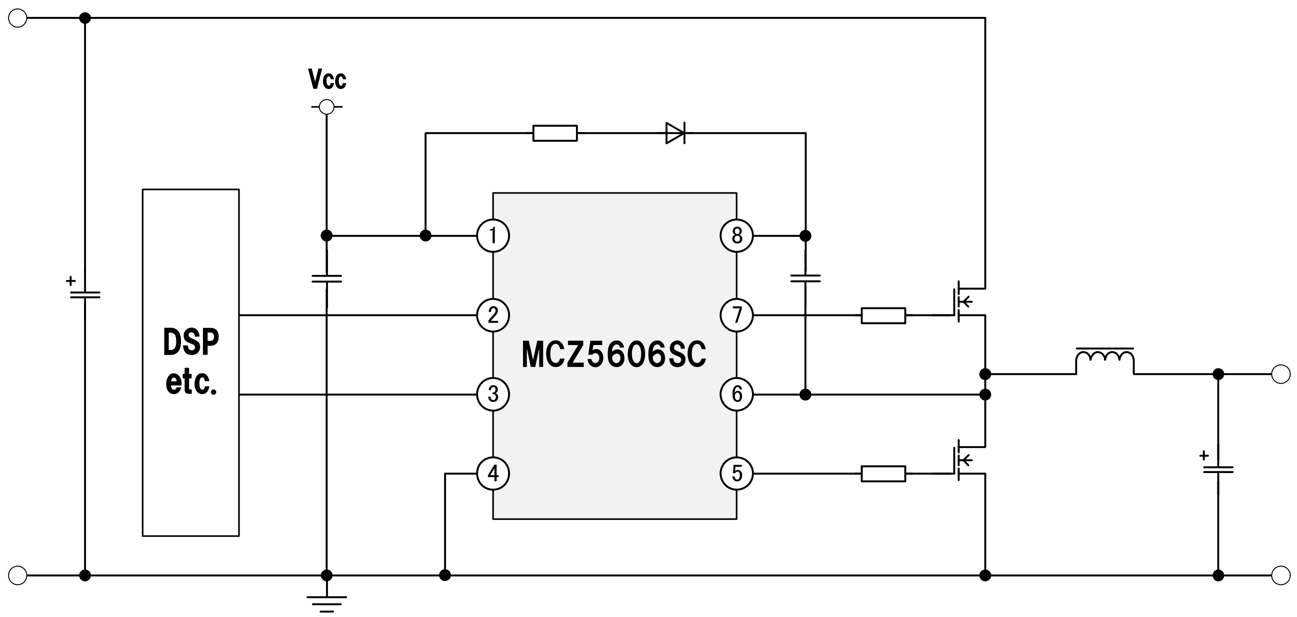
<Motor drive (general-purpose inverters, vacuum cleaners, air conditioning units, washing machines)>



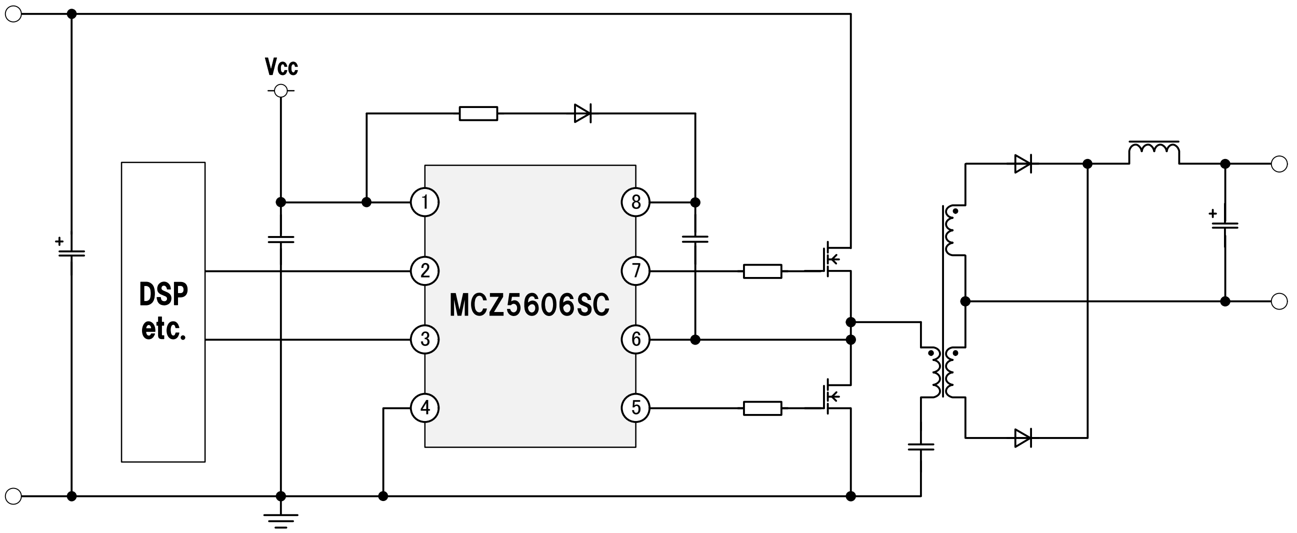
<Partial switching circuit>



<Chopper circuit>



<Half-bridge converter (current resonance circuit)>



MCZ5606SC/MCZ5607SC Application Note Version 1.0

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